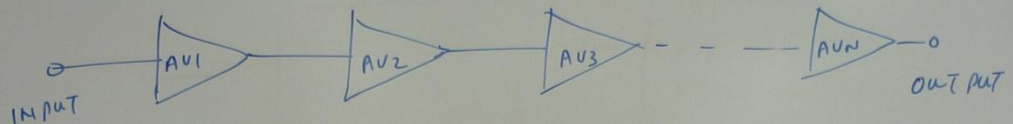
MULTI STAGE AMPLIFIERS



$$AV_T = AV_1 \times AV_2 \times AV_3 \times - - - AV_N$$

$$AV\,(dB) = 20 \log AV$$

$$AV_T(dB) = AV_1(dB_1) + AV_2(dB_2) + AV_3(dB_3) + - - - AV_N(dB_m)$$

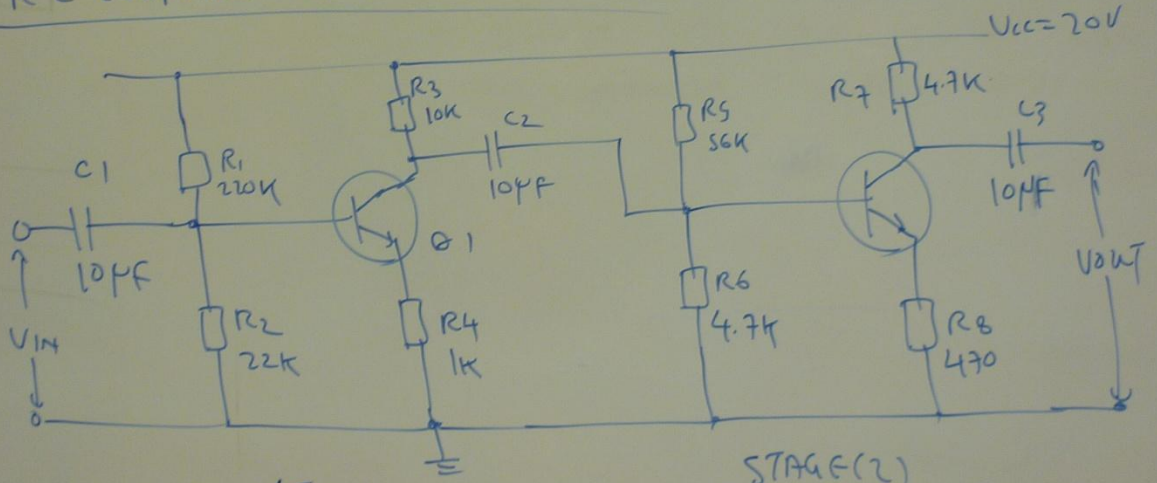
CASADING —— HIGHER GAIN
HIGH INPUT RESISTANCE, LOW OUTPUT RESISTANCE

COUPL
— RESIST
— DIRECT
— TRANS
— TUNE
— IN
RC COU
C1
10μF
VIN
OUT

COUPLING METHODS

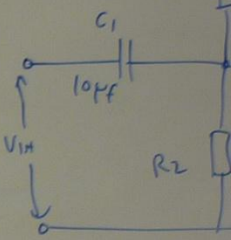
- RESISTANCE - CAPACITANCE (RC) COUPLING
- DIRECT COUPLING - (DC COUPLING)
- TRANSFORMER COUPLING
- TUNED TRANSFORMER COUPLING
- INDUCTANCE - CAPACITANCE COUPLING (LC COUPLING)

RC COUPLING FOR CE AMPLIFIER



OUT PUT WAVEFORM IS INPHASE WITH INPUT.

DIRECT couple



- NO BIASING
- HIGHER INP
- HIGHER GAI

Pb FOR ABO

(a) VB1 (6

(f) VE2

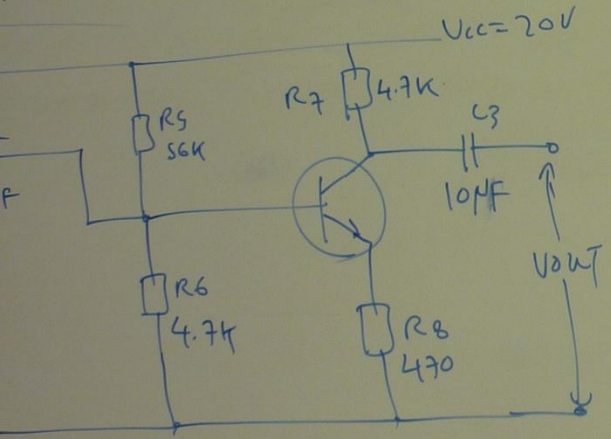
2C) COUPLING

NG)

NG

UPLING (LC COUPLING)

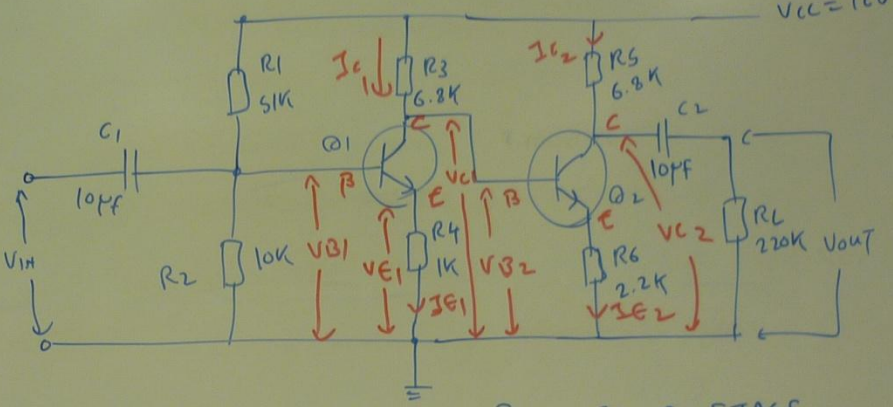
PLIFIER



STAGE(2)

IS INPHASE WITH INPUT.

DIRECT COUPLED AMPLIFIER



- NO BIASING CAPACITOR FOR SECOND STAGE
- HIGHER INPUT IMPEDANCE
- HIGHER GAIN.

Pb FOR ABOVE AMPLIFIER, CALCULATE

(a) V_{B_1} (b) V_{E_1} (c) I_{E_1} (d) I_{C_1} (e) V_{C_1}

(f) V_{E_2} (g) I_{E_2} (h) V_{C_2}

$V_{B_1} = V_{CC} \times$

$= 12 \times \frac{1}{10}$

$= 1.96$

$V_{E_1} = V_{B_1} - V$

$= 1.96 - 0.$

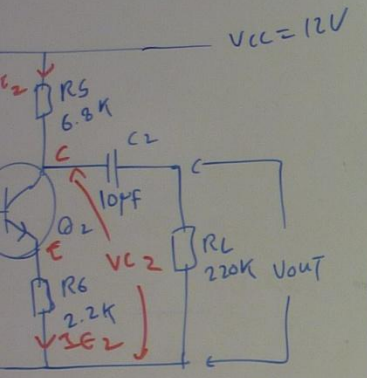
$V_{C_1} = V_{CC} -$

$I_{C_1} = I_{E_1} =$

$V_{C_1} = V_{CC} - I_C$

$= 12 - 1.$

$= 3.84$



SECOND STAGE

LCULATE

d) I_{C_1} (e) V_{C_1}

V_{C_2}

$$V_{B_1} = V_{cc} \times \frac{R_2}{R_1+R_2}$$

$$= 12 \times \frac{10}{10+51}$$

$$= 1.96V$$

$$V_{E_1} = V_{B_1} - V_{BE}$$

$$= 1.96 - 0.6 = 1.36V$$

$$V_{C_1} = V_{cc} - I_{C_1} R_3$$

$$I_{C_1} = I_{E_1} = \frac{V_{E_1}}{R_4}$$

$$= \frac{1.36}{1k}$$

$$= 1.36mA$$

$$V_{C_1} = V_{cc} - I_{C_1} R_3$$

$$= 12 - 1.36 \times 10^{-3} \times 6.8 \times 10^{3}$$

$$= 3.84V$$

$$V_{C_1} = V_{B_2}$$

$$V_{E_2} = V_{B_2} - V_{BE}$$

$$= 3.84 - 0.6$$

$$= 3.24V$$

$$I_{E_2} = \frac{V_{E_2}}{R_6}$$

$$= \frac{3.24}{2.2K}$$

$$= 1.6mA$$

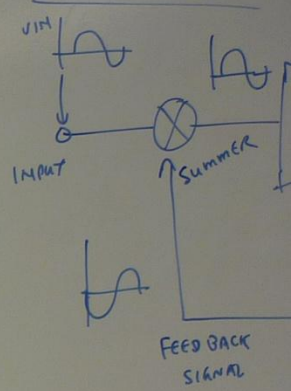
$$I_{E_2} = I_{C_2} = 1.6mA$$

$$V_{C_2} = V_{cc} - I_{C_2} \times R_S$$

$$= 12 - 1.6 \times 10^{-3} \times 6.8 \times 10^{3}$$

$$= 2.4V$$

FEED BACK



ADVANTAGES OF N

- REDUCED BUT S
- INCREASED IN PUT
- REDUCED OUTPUT
- LESS NOISE IN
- LESS DISTORTIO
- WIDER FREQUEN

DC FEED BACK

- DC VOLTAGE S

$V_{C_1} = V_{B_2}$

$V_{E_2} = V_{B_2} - V_{BE}$

$= 3.84 - 0.6$

$= 3.24\ V$

$I_{E_2} = \frac{V_{E_2}}{R_6}$

$= \frac{3.24}{2.2K}$

$= 1.6\ mA$

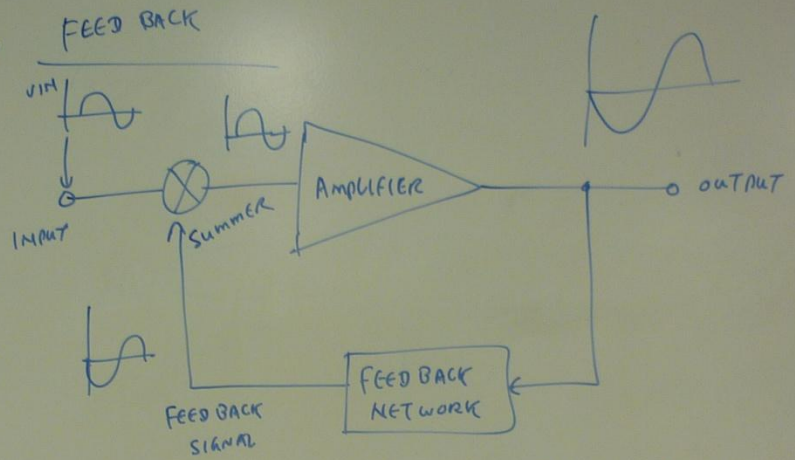
$I_{E_2} = I_{C_2} = 1.6\ mA$

$V_{C_2} = V_{CC} - I_{C_2} \times R_5$

$= 12 - 1.6 \times 10^{-3} \times 6.8 \times 10^{3}$

$= 2.4V$

FEED BACK



ADVANTAGES OF NEGATIVE FEED BACK

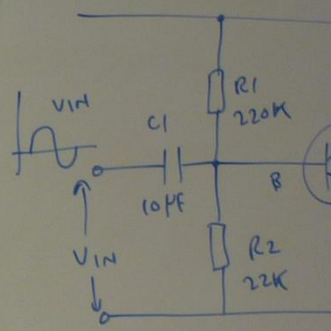
- REDUCED BUT STABILISED GAIN
- INCREASED INPUT RESISTANCE
- REDUCED OUTPUT RESISTANCE
- LESS NOISE IN OUTPUT SIGNAL
- LESS DISTORTION IN OUTPUT SIGNAL
- WIDER FREQUENCY RESPONSE.

AC FEED BACK

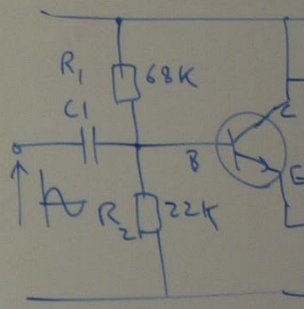
DC FEED BACK

- DC VOLTAGE STABILIZING

EMITTER RESISTOR



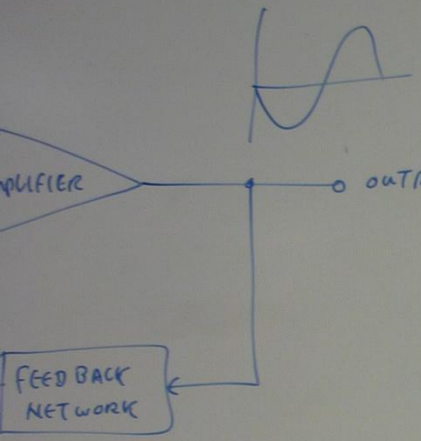
CURRENT DERIVE



DC & AC F

R_5 - LOAD FOR

RESISTANCE FO



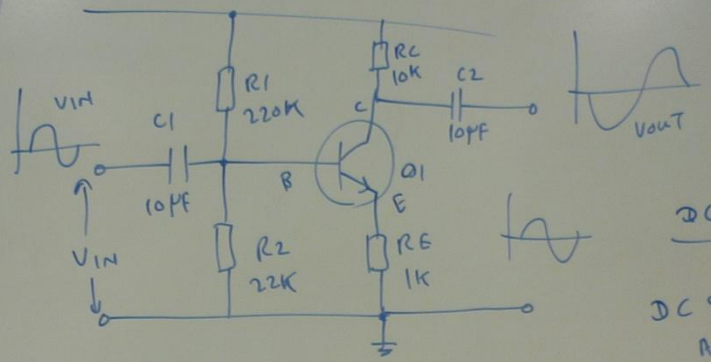
A TIVE FEED BACK

BILISED GAIN
ESISTANCE
ESISTANCE
T PUT SIGNAL
N OUTPUT SIGNAL
RESPONSE.

BILIZING

AC FEED BACK

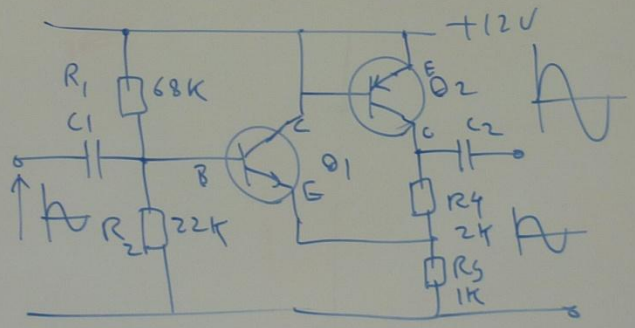
EMITTER RESISTOR AS FEED BACK



CURRENT DERIVED FEED BACK.

DC FEED BACK

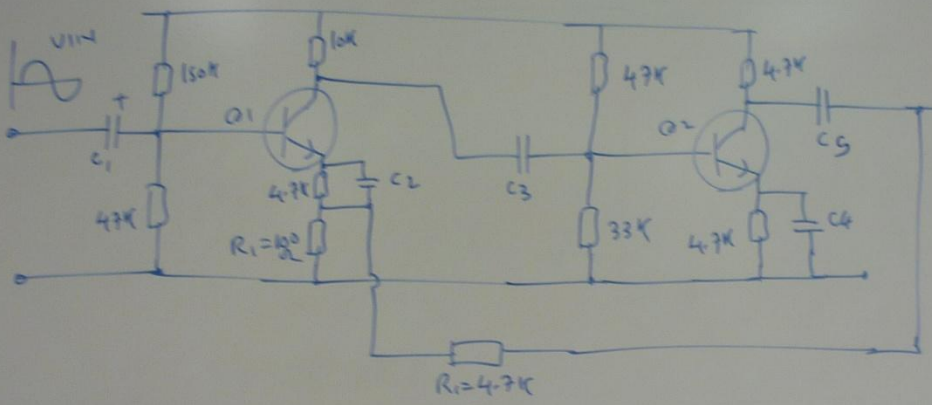
DC STABILITY CAN BE ACHIEVED



DC & AC FEED BACK.

R_5 - LOAD FOR Q_2, EMITTER FEED BACK RESISTANCE FOR Q_1.

VOLTAGE DERIVED FEED BACK



C_5 – DC ISOLATION

C_2 – BY PASS

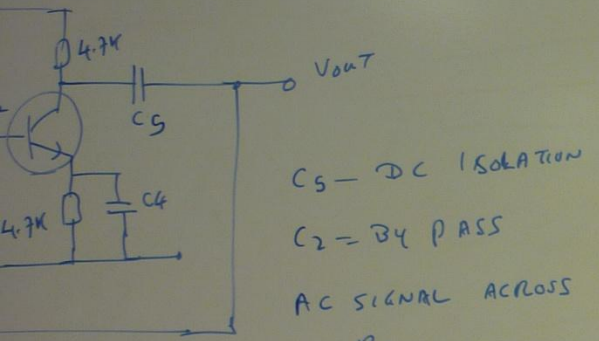
AC SIGNAL ACROSS R_1

FEED BACK GAIN $A_{Vf} = \frac{R_f}{R_1} + 1$

BENEFIT OF VOLTAGE FEED BACK

– LOWER THE CIRCUIT GAIN AND STABILIZE IT
– INCREASE THE INPUT RESISTANCE
– DECREASE THE OUTPUT RESISTANCE
– PROVIDE ALL BENEFITS OF NEGATIVE FEED BACK.

} AC FEED BACK



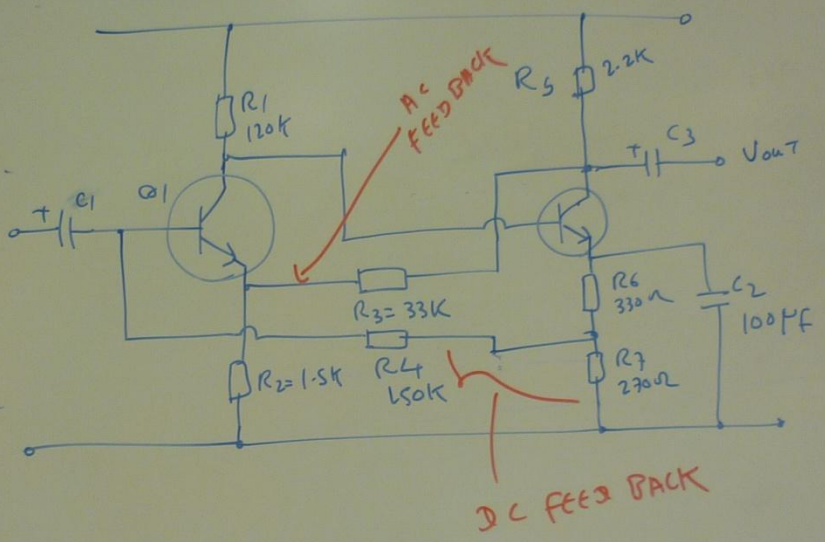
C_5 — DC ISOLATION

C_2 = BY PASS

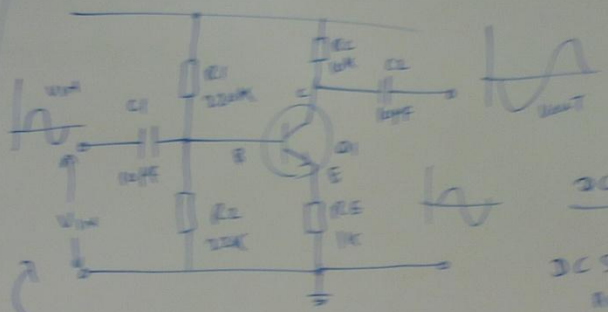
AC SIGNAL ACROSS R_1

AC FEED BACK

EXAMPLES OF AC & DC FEED BACK



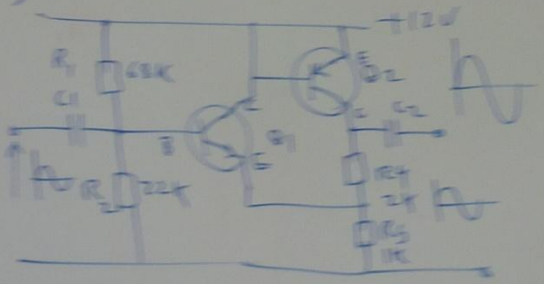
EMITTER RESISTOR AS FEED BACK



DC FEEDBACK

DC STABILITY CAN BE ACHIEVED

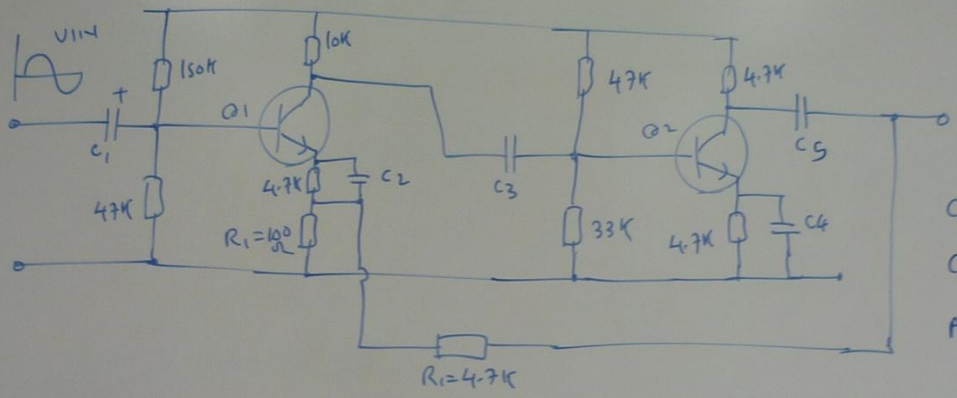
CURRENT DERIVED FEED BACK



DC & AC FEEDBACK.

R_4 - LOAD FOR Q_2, EMITTER FEEDBACK RESISTANCE FOR Q_1.

VOLTAGE DERIVED FEED BACK



C_5 — DC ISOLATION

C_2 — BY PASS

AC SIGNAL ACROSS R_1

↑ R_f

FEED BACK GAIN $A_{Vf} = \frac{R_f}{R_1} + 1$

BENEFIT OF VOLTAGE FEED BACK

— LOWER THE CIRCUIT GAIN AND STABILIZE IT

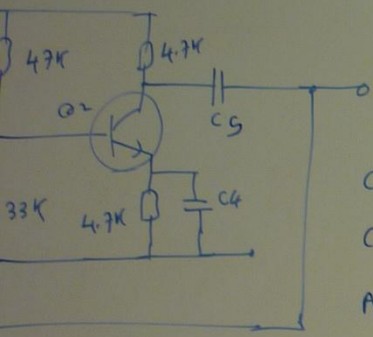
— INCREASE THE INPUT RESISTANCE

— DECREASE THE OUTPUT RESISTANCE

— PROVIDE ALL BENEFITS OF NEGATIVE FEED BACK.

↳ — AC FEED BACK

EXAMPL



C_5 — DC ISOLATION

C_2 = BY PASS

AC SIGNAL ACROSS R_1

$-+1$

ABILIZE IT

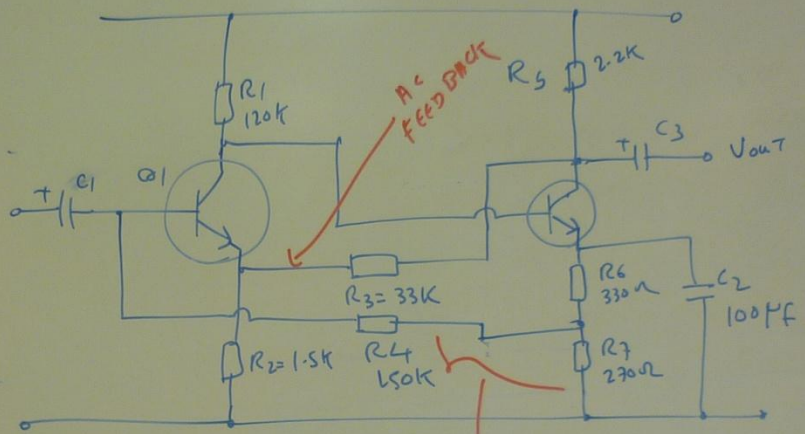
CE

TANCE

GATIVE FEED BACK.

AC FEED BACK

EXAMPLES of AC & DC FEED BACK



FIELD EFFE

BJT - TRANSISTOR

FET - TRANSISTOR -

FET J

M

J FET

DRA

GATE (G)

N

P

A

CHANNEL

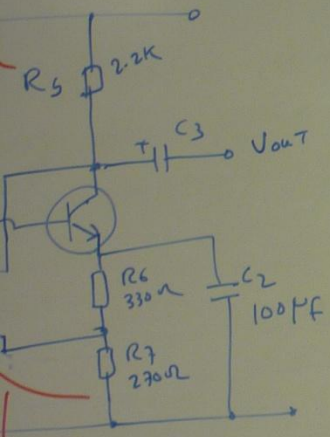
N-CHANNEL

SOUR

G

N C

FEED BACK



C FEED BACK

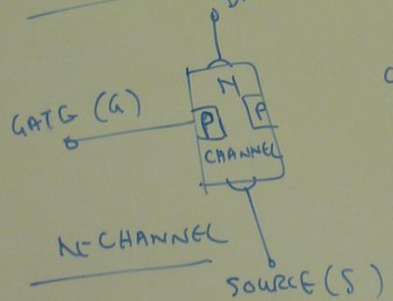
FIELD EFFECT TRANSISTORS

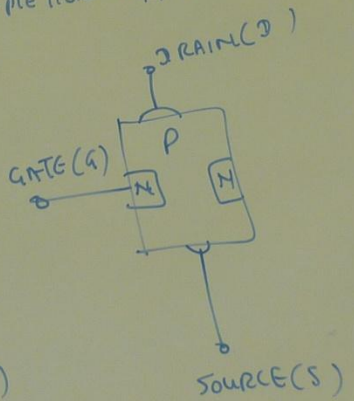
BJT - TRANSISTOR - THE JUNCTION IS OPERATED WITH REVERSE BIAS

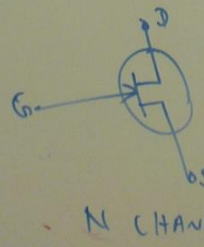
FET - TRANSISTOR - FET IS A VOLTAGE OPERATED DEVICE.

FET
- JFET — JUNCTION FIELD EFFECT TRANSISTOR
- MOSFET — METAL OXIDE SILICON FIELD EFFECT TRANSISTOR
  - DEPLETION TYPE
  - ENHANCEMENT TYPE

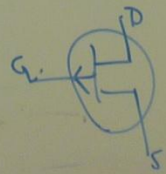
J FET

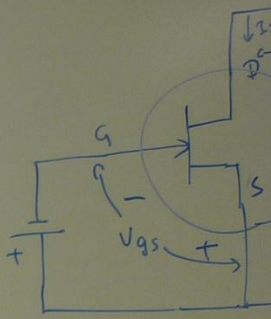






P-CHANNEL





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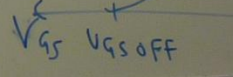
WHEN VGS

IDSS - DR



IS OPERATED WITH REVERSE BIAS

TAGE OPERATED DEVICE.

N FIELD EFFECT TRANSISTOR

OXIDE SILICON FIELD EFFECT TRANSISTOR

ENHANCEMENT TYPE

YPE

DRAIN(D)

P

N

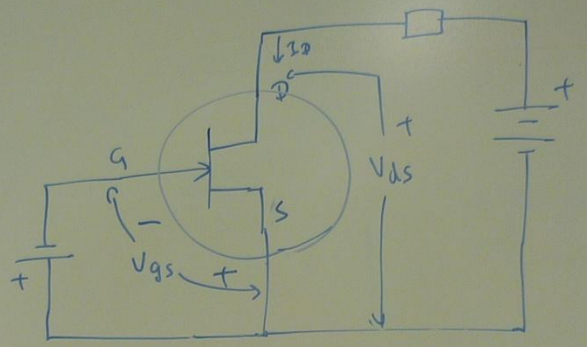
SOURCE(S)

HANNEL

D

P-CHANNEL

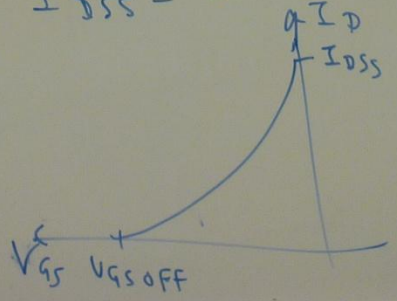
S



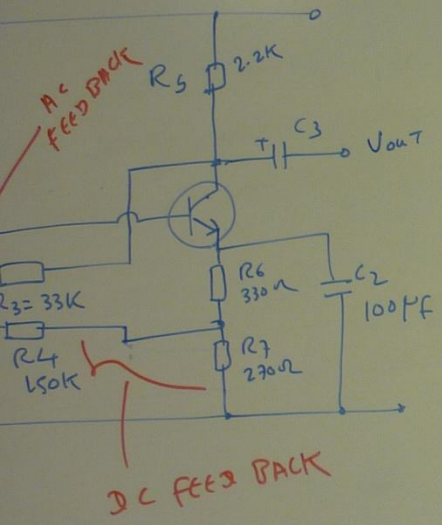
THE HIGHER THE VALUE OF V_{GS}, THE GREATER THE DEPTH OF THE FIELD AND THE HIGHER THE RESISTANCE OFFERED TO THE CURRENT FLOWING FROM DRAIN TO SOURCE TERMINAL.

WHEN V_{GS} IS ZERO → CURRENT FLOWS

I_{DSS} – DRAIN CURRENT FLOWS WHEN $V_{GS}=0$



& DC FEED BACK



FIELD EFFECT TRANSISTORS

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- JFET — JUNCTION FIELD EFFECT TRANSISTOR
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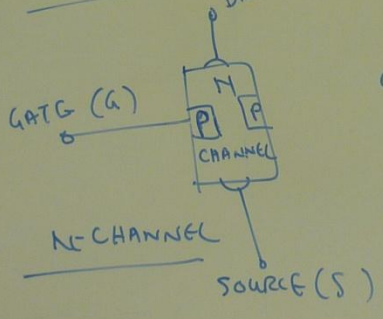
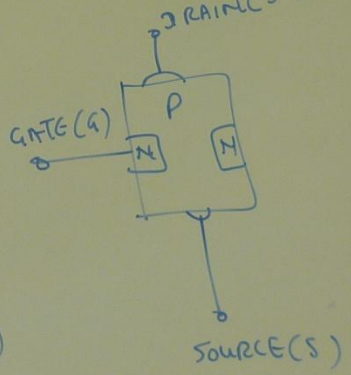
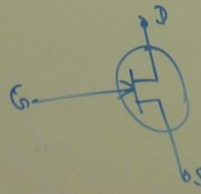
  - DEPLETION TYPE
  - ENHANCEMENT TYPE

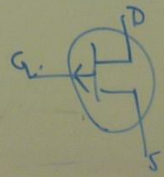
JFET

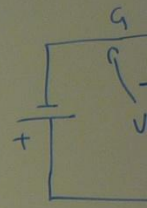






P-CHANNEL





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WHEN

I_{DS}

V_{GS} V_G

... IS OPERATED WITH REVERSE BIAS

...OLTAGE OPERATED DEVICE

...ION FIELD EFFECT TRANSISTOR

... OXIDE SILICON FIELD EFFECT TRANSISTOR

ENHANCEMENT TYPE

...YPE

DRAIN(D)

P

N N

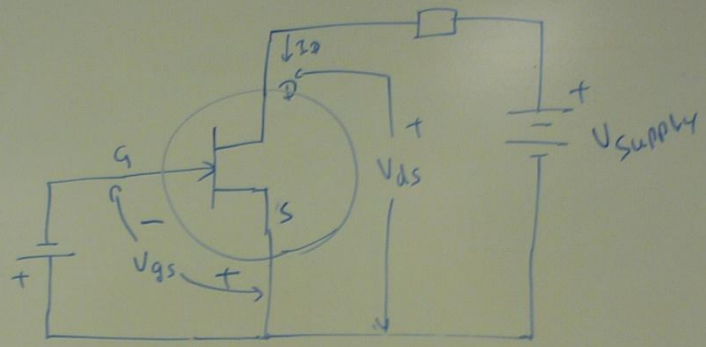
SOURCE(S)

...CHANNEL

P

P-CHANNEL

S



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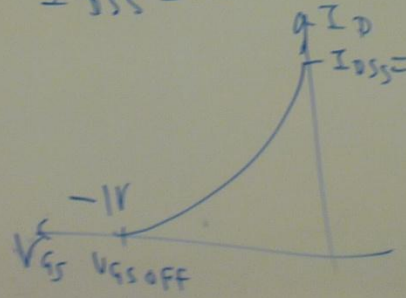
WHEN V_{GS} IS ZERO → CURRENT FLOWS

I_{DSS} – DRAIN CURRENT FLOWS WHEN $V_{GS}=0$

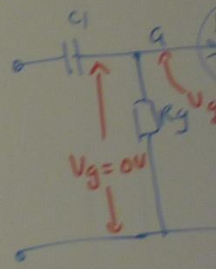


DC CONDITION OF

$V_{ds} = \frac{1}{2} V_{supply}$

V_{gs} – REVERSED B...

Id



Pb FOR THE A...

$V_{gs} = -1V$

(a) THE V...

(b) R_d

(c) MUT...

+
V_{SUPPLY}

gs, THE
AND
ERED TO
DRAIN

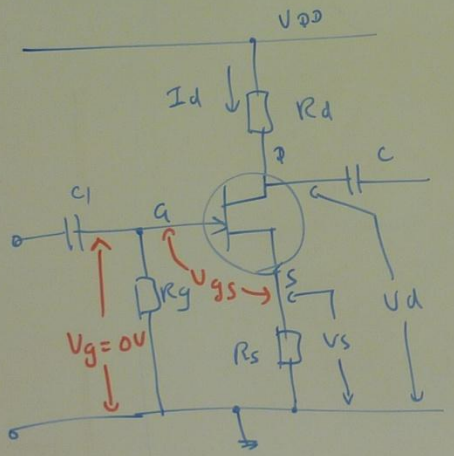
RRENT FLOWS

ows WHEN $V_{GS}=0$

DC CONDITION OF JFET

$V_{ds} = \frac{1}{2} V_{supply}$

V_{gs} – REVERSED BIAS



$I_D = \frac{I_{DSS}}{2}$

$V_{gs} = -I_d R_S$

$R_S = \frac{V_{gs}}{R_D}$

$g_m = \frac{I_d}{V_{gs}}$

$V_D = V_{DD} - I_d R_d$

R_g = 1 mΩ (OR) LESS
(FOR JFET)

Pb FOR THE ABOVE CIRCUIT DIAGRAM, $V_{dd} = 10V$,
$V_{gs} = -1V$ $I_{DSS} = 10mA$ CALCULATE
(a) THE VALUE OF R_S TO CORRECTLY BIAS THE CIRCUIT
(b) R_d
(c) MUTUAL CONDUCTANCE g_m (amp/volt)

(a) $I_D = \frac{I_{DSS}}{2} =$

$R_S = \frac{V_{gs}}{I_D} =$

(b) $V_D = V_{DD} - I$

$I_d R_d = V_{DD}$

$R_d = \frac{V_{DD}}{}$

$= \frac{10}{}$

$= \frac{10}{}$

$=$

(c) $g_m = \frac{I_D}{V_{gs}}$

$$I_D = \frac{I_{DSS}}{2}$$

$$V_{gs} = -I_d R_S$$

$$R_S = \frac{V_{gs}}{R_D} \qquad g_m = \frac{I_d}{V_{gs}}$$

$$V_D = V_{DD} - I_d R_d$$

$R_g = 1\ M\Omega$ (OR) LESS
(FOR JFET)

T DIAGRAM, $V_{dd} = 10V$,
10mA CALCULATE
TO CORRECTLY BIAS THE CIRCUIT

NCE g_m (amp/volt)

(a) $I_D = \frac{I_{DSS}}{2} = \frac{10\ mA}{2} = 5\ mA$

$$R_S = \frac{V_{gs}}{I_D} = \frac{1}{5\ mA} = 0.2 \times 10^3\ \Omega = 200\ \Omega$$

(b) $V_D = V_{DD} - I_d R_d$

$$I_d R_d = V_{DD} - V_D$$

$$R_d = \frac{V_{DD} - V_D}{I_d}$$

$$= \frac{10 - \frac{V_{DD}}{2}}{5\ mA}$$

$$= \frac{10 - \frac{10}{2}}{5 \times 10^{-3}}$$

$$= \frac{5}{5 \times 10^{-3}} = 1\ k\Omega$$

(c) $g_m = \frac{I_D}{V_{gs}} = \frac{5\ mA}{1V} = 5\ mA/V$

(a) $I_D = \frac{I_{DSS}}{2} = \frac{10\,mA}{2} = 5\,mA$

$R_S = \frac{V_{GS}}{I_D} = \frac{1}{5\,mA} = 0.2 \times 10^3\,\Omega = 200\,\Omega$

(b) $V_D = V_{DD} - I_d R_d$

$I_d R_d = V_{DD} - V_D$

$R_d = \frac{V_{DD} - V_D}{I_d}$

$= \frac{10 - \frac{V_{DD}}{2}}{5\,mA}$

$= \frac{10 - \frac{10}{2}}{5 \times 10^{-3}}$

$= \frac{5}{5 \times 10^{-3}} = 1\,k\Omega$

(c) $g_m = \frac{I_D}{V_{GS}} = \frac{5\,mA}{1V} = 5\,mA/V$

MOSTIC

MOS FET

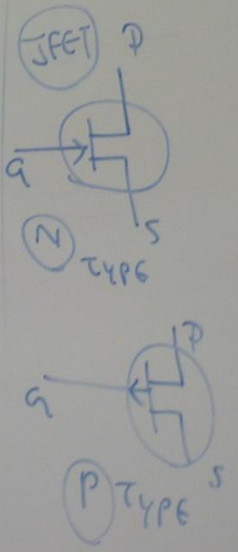
THE MOSFET IS SIMILAR CONSTRUCTION TO JFET EXCEPT A VERY THIN LAYER OF SILICON OXIDE IS PLACED BETWEEN GATE AND CHANNEL

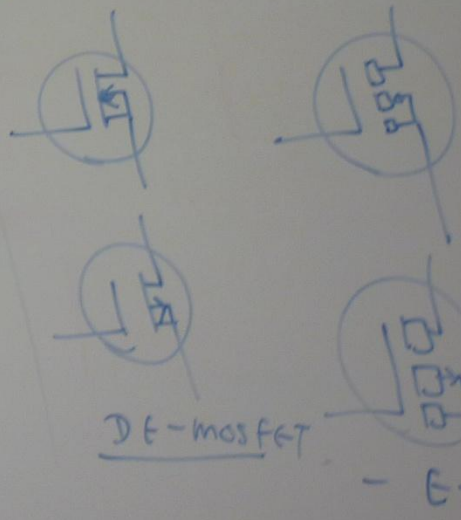
DE-MOSFET - DEPLETION ENHANCEMENT MODE

DESIGNED TO OPERATE WITH GATE-SOURCE VOLTAGE REVERSED BIAS

E-MOSFET - ENHANCEMENT MODE MOSFET -

DESIGNED TO OPERATE GATE-SOURCE VOLTAGE FORWARD BIAS.





J-FET AMPLIFIER

THE J FET AMPLIFIER IS SIMPLER THAN BJT . IT USES LESS COMPONENT AND VOLTAGE OPERATED.

THE GATE-SOURCE VOLTAGE OF FET CONTROLS IT'S DRAIN CURRENT

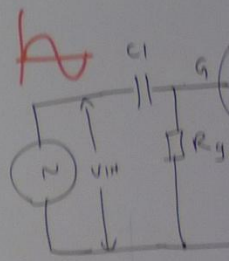
(IN BJT- BASE CURRENT CONTROLS COLLECTOR CURRENT)

- INPUT IMPEDANCE of FET IS HIGHER THAN BJT

CD - COMMON DRAIN , CS - COMMON SOURCE.

JFET	—	BJT
CD		CE
CS	—	EMITTER FOLLOWER

JFET - CS



AC CONDITION

V_{IN} ↑

VS CONST

Id ↑

Vd ↓

∴ OUT P

PLER THAN BJT . IT USES LESS

ET CONTROLS ITS DRAIN CURRENT

S COLLECTOR CURRENT)

ER THAN BJT

MMON SOURCE.

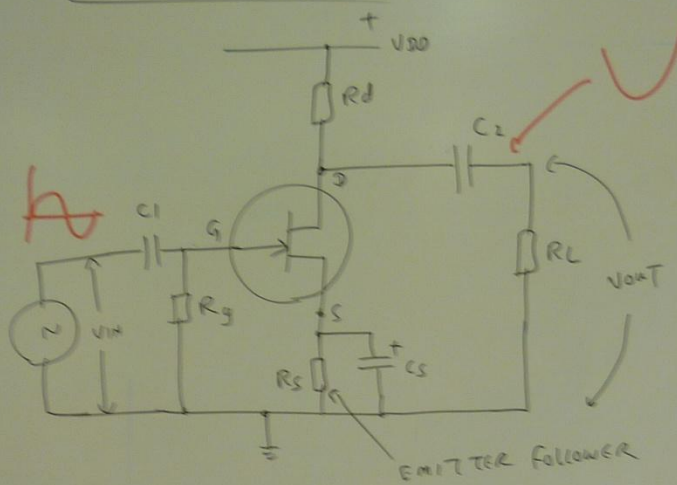
IT

E

NITTER

LOWER

JFET - CS AMPLIFIER



OUT PUT IS 180° OUT OF PHASE WITH INPUT.

AC CONDITION

$V_{IN} \uparrow \rightarrow V_g \uparrow$

V_S CONSTANT

$I_d \uparrow$

$V_d \downarrow$

∴ OUT PUT DECREASES.

INCREASE IN INPUT CAUSES DECREASES IN OUT PUT

(180° OPPOSITE)

$A_V =$ $\frac{g_m}{1+}$

$g_m =$ MUTUA

$R_d =$ VALUE

$R_L =$ VALUE

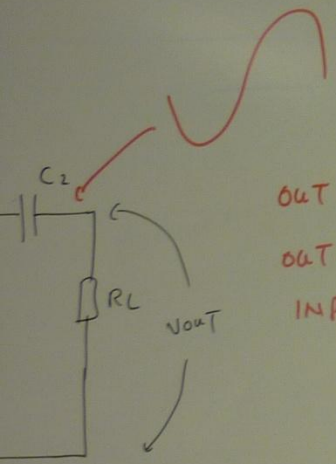
$R_S =$ VALU

$A_V = g_m (R_d$

$A_V = g_m R_d$

$r_{in} = R_g$

$r_{out} = R_d$



OUT PUT IS 180° OUT OF PHASE WITH INPUT.

7TER FOLLOWER

INCREASE IN INPUT CAUSES DECREASES IN OUT PUT

(180° OPPOSITE)

$$A_V = \frac{g_m (R_d \,||\, R_L)}{1 + g_m R_S}$$

g_m = MUTUAL CONDUCTANCE AMP/VOLT

R_d = VALUE OF DRAIN RESISTOR

R_L = VALUE OF LOAD RESISTOR

R_S = VALUE OF UNBYPASSED SOURCE RESISTOR.

$A_V = g_m (R_d \,||\, R_L)$ (RS IS BYPASSED)

$A_V = g_m R_d$ (RS IS BYPASSED, NO LOAD RESISTOR CONNECTED)

$r_{in} = R_g$

$r_{out} = R_d$

J-FET AMPLIFIER

THE J FET AMPLIFIER IS SIMPLER THAN BJT. IT USES LESS COMPONENT AND VOLTAGE OPERATED.

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J FET	BJT
CD	CE
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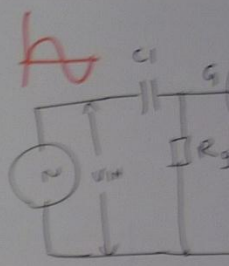
J FET - CS



AC CONDITION

U_{in} ↑ →

V_S CONST

I_d ↑

V_d ↓

∴ OUT PU

LIFIER

SIMPLER THAN BJT . IT USES LESS

ATED.

FET CONTROLS IT'S DRAIN CURRENT

TROLS COLLECTOR CURRENT)

HIGHER THAN BJT

COMMON SOURCE.

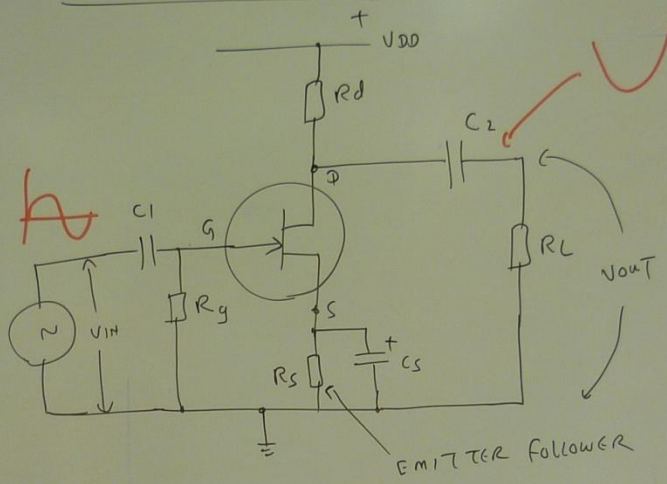
BJT

CE

EMITTER

FOLLOWER

JFET - CS AMPLIFIER



OUT PUT IS 180° OUT OF PHASE WITH INPUT.

AC CONDITION

$V_{IN} \uparrow \rightarrow V_g \uparrow$

V_S CONSTANT

$I_d \uparrow$

$V_d \downarrow$

i. OUT PUT DECREASES.

INCREASE IN INPUT CAUSES DECREASES IN OUT PUT

(180° OPPOSITE)

$A_V =$

$g_m =$

$R_d =$ VA

$R_L =$ VA

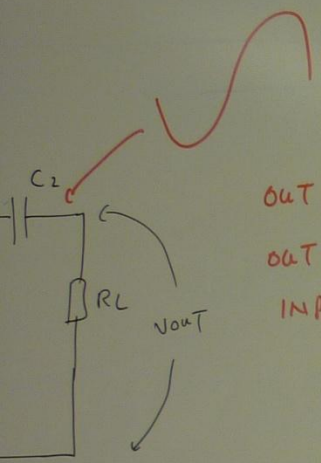
$R_S =$ V

$A_V = g_m$ (R

$A_V = g_m$

$r_{in} = R_g$

$r_{out} = R$



OUT PUT IS 180° OUT OF PHASE WITH INPUT.

TTER FOLLOWER

INCREASE IN INPUT CAUSES DECREASES IN OUT PUT

(180° OPPOSITE)

$$A_V = \frac{g_m (R_d \,||\, R_L)}{1 + g_m R_S}$$

pb

g_m = MUTUAL CONDUCTANCE AMP/VOLT

R_d = VALUE OF DRAIN RESISTOR

R_L = VALUE OF LOAD RESISTOR

R_S = VALUE OF UN BYPASSED SOURCE RESISTOR.

$A_V = g_m (R_d \,||\, R_L)$ (R_S IS BYPASSED)

$A_V = g_m R_d$ (R_S IS BYPASSED, NO LOAD RESISTOR CONNECTED)

$r_{in} = R_g$

$r_{out} = R_d$

FOR THE

CALCULA

(a)

(b)

(c)

(d)

Pb

FOR THE GIVEN JFET CIRCUIT, $g_m = 3\ mA/V$

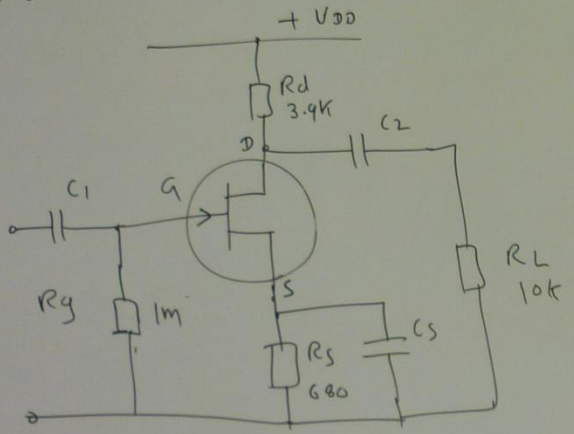
CALCULATE

(a) VOLTAGE GAIN OF THE CIRCUIT

(b) INPUT RESISTANCE

(c) OUT PUT RESISTANCE

(d) VOLTAGE GAIN IF BY PASS CAPACITOR IS REMOVED



$$Rd \,||\, RL = \frac{Rd\,RL}{Rd+RL}$$

(a) $$A_V = \frac{g_m\,(Rd\,||\,RL)}{1+g_m R_S}$$

$$= \frac{g_m \times \frac{Rd\,RL}{Rd+RL}}{1+g_m R_S}$$

$$= \frac{3\times10^{-3} \times \frac{3.9\times10}{3.9+10}}{1+3\times10^{-3}\times 680}$$

$$= 2.76$$

(b) $r_{in} = r_g = 1\ M\Omega$

(c) $r_{out} = R_d = 3.9\ k\Omega$

(d) $A_V = g_m(Rd\,||\,RL)$

$$= 3\times10^{-3}\left(\frac{3.9\times10}{3.9+10}\right) \approx 8.4$$

= 3 mA/V

...OR IS REMOVED

RL
10k

(a) $A_V = \dfrac{g_m (R_d || R_L)}{1 + g_m R_s}$

$= \dfrac{g_m \times \dfrac{R_d R_L}{R_d + R_L}}{1 + g_m R_s}$

$= \dfrac{3 \times 10^{-3} \times \dfrac{3.9 \times 10}{3.9 + 10}}{1 + 3 \times 10^{-3} \times 680}$

$= 2.76$

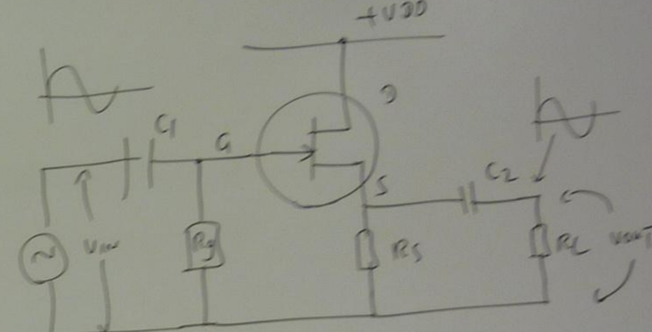
(b) $r_{in} = r_g = 1\ M\Omega$

(c) $r_{out} = R_d = 3.9k\Omega$

(d) $A_V = g_m (R_d || R_L)$

$= 3 \times 10^{-3} \left(\dfrac{3.9 \times 10}{3.9 + 10} \right) \approx 8.4$

COMMON DRAIN JFET AMPLIFIER



- HIGH INPUT RESISTANCE
- LOW OUTPUT RESISTANCE
- VOLTAGE GAIN $\simeq 1$

$A_V = \dfrac{g_m (R_s || R_L)}{1 + g_m R_s}$

$r_{in} = R_g$

$r_{out} = \dfrac{R_s}{1 + g_m R_s}$

- APPLICAT...

TO ...

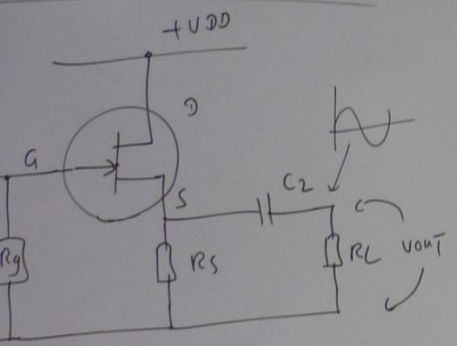
Pb

FOR TH...

(a)

(b)

AIN JFET AMPLIFIER



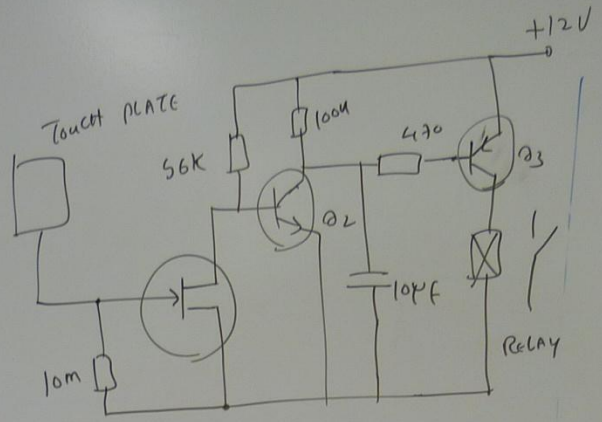
PUT RESISTANCE

PUT RESISTANCE

GAIN ≃ 1

$$\frac{g_m (R_s \| R_L)}{1 + g_m R_s}$$

$$= \frac{R_g}{\frac{R_s}{1 + g_m R_s}}$$

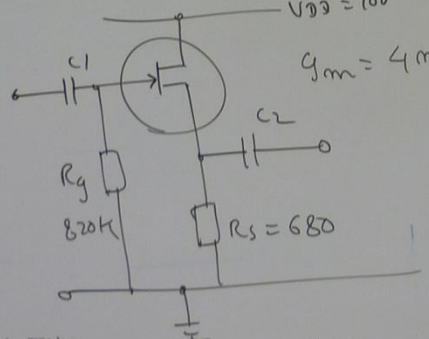


– APPLICATION

TOUCH SCREEN TECHNOLOGY

COMPUTER TOUCH SWITCH

Pb



$g_m = 4\,mA/V$

FOR THE GIVEN CIRCUIT, CALCULATE

(a) VOLTAGE GAIN

(b) INPUT RESISTANCE

(c) OUT PUT RESISTANCE

(a) $A_V \simeq 1$

(b) $r_{in} = R_g = 820K$

(c) $r_{OUT} = \frac{R_S}{1 + g_m R_S}$

$= \frac{680}{1 + 4 \times 10^{-3} \times 680}$

$= 182\,\Omega$