DIGITAL SIGNAL PROCESSING

DIGITAL THEORY

ANALOG: A SYSTEM CAPABLE OF PRODUCING AN OUTPUT THAT IS CONTINUOUSLY VARIABLE

DIGITAL - A SYSTEM THAT PRODUCES AN OUTPUT OF TWO STATES ONLY.

CMOS : COMPLEMENTARY METAL OXIDE SILICON
N & P CHANNEL MOS FETs.
LOW SPEED / LOW POWER CONSUMPTION

TTL - TRANSISTOR TRANSISTOR LOGIC
HIGH SPEED

DTL - DIODE TRANSISTOR LOGIC
A COMBINATION OF TRANSISTORS AND D
IMPLEMENT THE REQUIRED FUNCTION

HTL - HIGH THRESHOLD LOGIC
HIGH NOISE IMMUNITY
ESPECIALLY USEFUL IN INDUSTRIAL
CONTROL APPLICATIONS.

ECL - EMITTER COUPLED LOGIC.
VERY SHORT GATE PROPAGATION
DELAY TIME.

TORS AND DIODES TO

FUNCTION

DUSTRIAL

AGATION

LOGIC → COMBINATIONAL LOGIC – OUTPUT CAN BE PREDICTED AT ANY TIME PROVIDED THAT INPUTS ARE KNOWN

→ SEQUENTIAL LOGIC – TIME + MEMORY IN TO SYSTEM

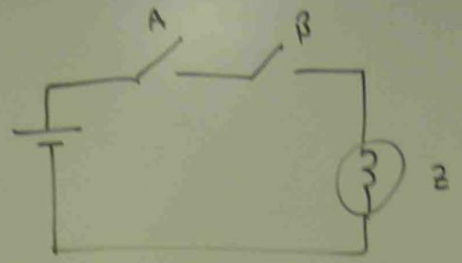
SYNCHRONOUS LOGIC – MASTER (CLOCK – SQUARE WAVE GENERATOR)

– PROVIDE REGULAR TIMING (OR) CLOCKING PULSES.

ASYNCHRONOUS LOGIC – EVENTS OCCUR AFTER THE P/REVIOUS EVENT IS COMPLETED.

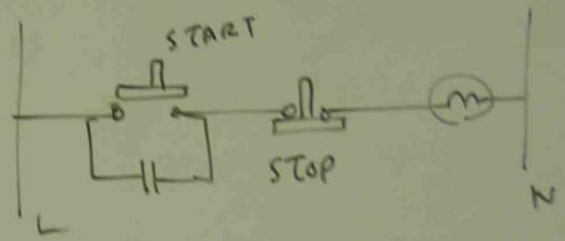
– TO SETUP CHAIN REACTION OF EVENTS.

AND GATE

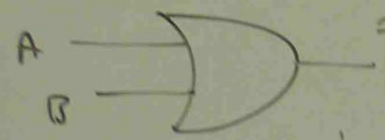


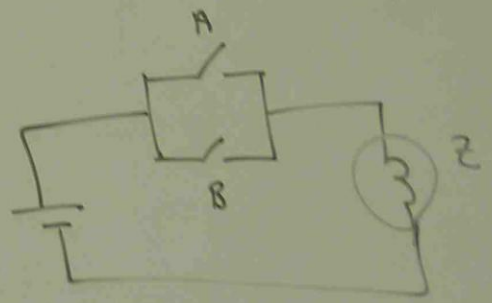
TRUTH TABLE

A	B	Z
0	0	0
0	1	0
1	0	0
1	1	1



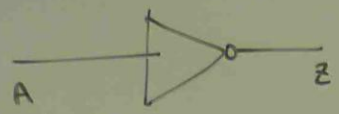
OR GATE



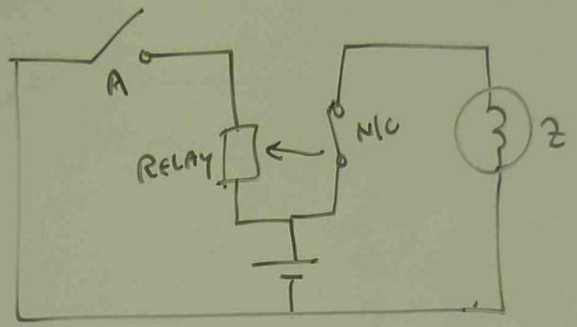


A	B	Z
1	0	1
0	1	1
1	1	1
0	0	0

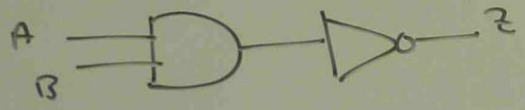
NOT GATE (INVERTER)



A	Z
0	1
1	0



NAND GATE



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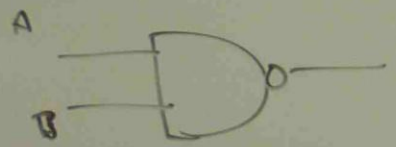
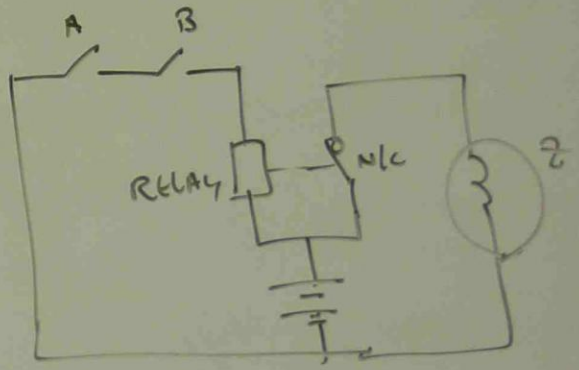
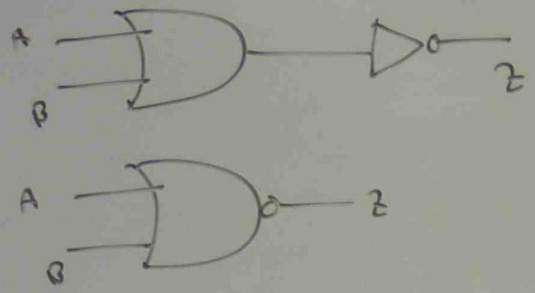


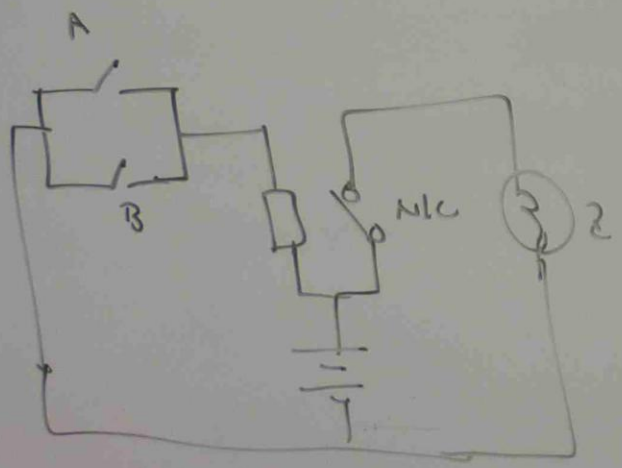
A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0



NOR GATE

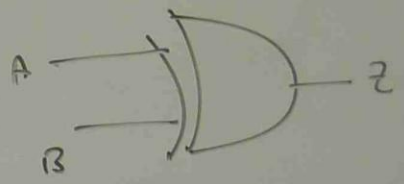


A	B	Z
0	0	1
0	1	0
1	0	0
1	1	0



EX-OR

A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0



GATE	CMOS	TTL
NOT INVERTOR	4069	7404

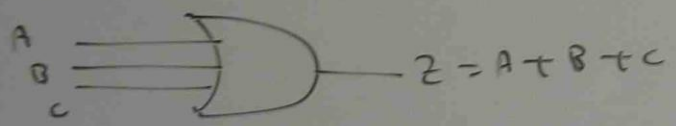
ICs

GATE TYPE	COMS	TTL
AND	4081	7408
OR	4071	7432
NAND	4011, 4023 4012, 4068	7400, 7410 7420, 7430
NOR	4001	7402
EX OR	4070	7486
EX NOR	4077	9386

BOOLEAN ALGEBRA

AND

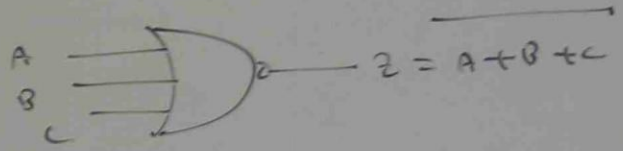
OR



NOT

NAND

NOR



BOOLEAN POSTULATES

$0 \cdot 0 = 0$

$1 + 1 = 1$

$0 + 0 = 0$

$1 \cdot 1 = 1$

$1 \cdot 0 = 0 \cdot 1 = 0$

$1 + 0 = 0 + 1$

$A + 0 = A$

$A \cdot 0 = 0$

$A + 1 = 1$

$A + A = A$

$A \cdot A = A$

$A + \overline{A} = 1$

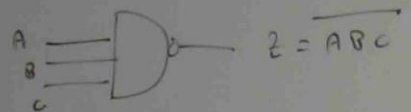
$A \cdot \overline{A} = 0$

$A + B = B + A$

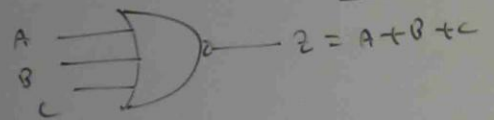
$\overline{\overline{A}} = A$

$A \cdot B = B \cdot A$

NAND



NOR



BOOLEAN POSTULATES

$0.0 = 0$

$1+1 = 1$

$0+0 = 0$

$1.1 = 1$

$1.0 = 0.1 = 0$

$1+0 = 0+1 = 1$

$A+0 = A$

$A.0 = 0$

$A+1 = 1$

$A+A = A$

$A.A = A$

$A+\overline{A} = 1$

$A.\overline{A} = 0$

$A+B = B+A$

$\overline{\overline{A}} = A$

$A.B = B.A$

DEMORGAN THEOREM

$$A+B = \overline{\overline{A}.\overline{B}}$$

$$(A.B).(C+D) = \overline{(\overline{A}+\overline{B})+(\overline{C+D})}$$

EQUIVALENT

USE NAND

GATE	NAND
NOT	
AND	
OR	
NAND	
NOR	

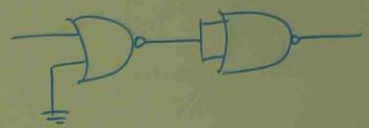
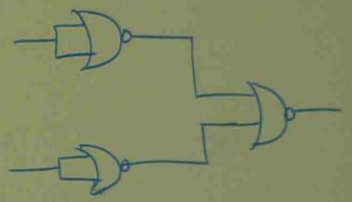
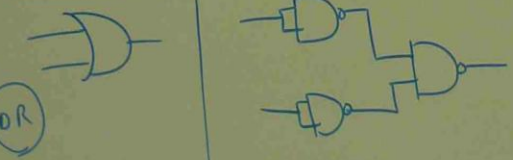
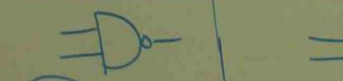
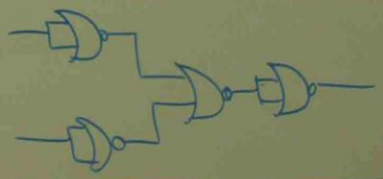
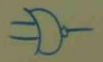
DEMORGAN THEOREM

$$A + B = \overline{\overline{A} \cdot \overline{B}}$$

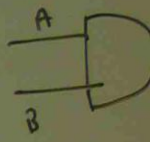
$$(A \cdot B) \cdot (C + D) = (\overline{A} + \overline{B}) + \overline{(C + D)}$$

EQUIVALENT GATES

USE NAND & NOR GATES TO GET AND, OR, NOR, EX OR NOT FUNCTIONS.

GATE	NAND EQUIVALENT	NOR EQUIVALENT
NOT		
AND		
OR		
NAND		
NOR		

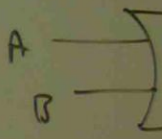
AND



TRUTH

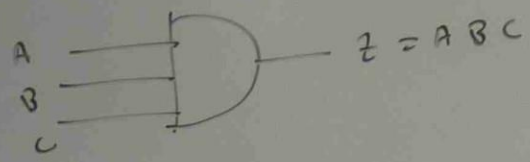
A	B
0	0
0	1
1	0
1	1

OR

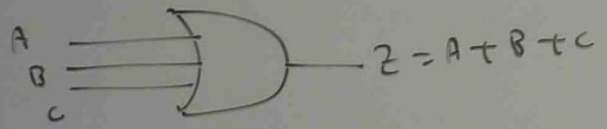


BOOLEAN ALGEBRA

AND

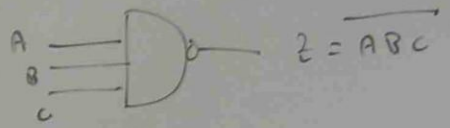


OR

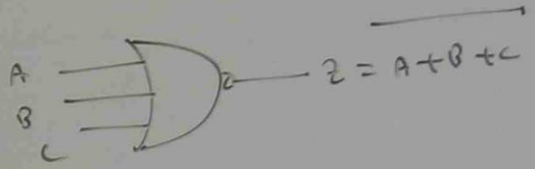


NOT

NAND



NOR



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$A+A = A$

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$A+\overline{A} = 1$

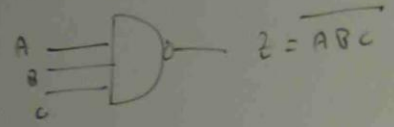
$A.\overline{A} = 0$

$A+B = B+A$

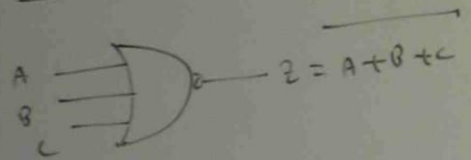
$\overline{\overline{A}} = A$

$A.B = B.A$

NAND



NOR



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$A.\overline{A} = 0$

$A+B = B+A$

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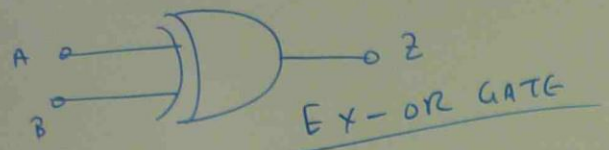
EQUIVALENT GA

USE NAND &

GATE	NAND EQUI
NOT	
AND	
OR	
NAND	
NOR	

ADDER CIRCUIT



EX-OR GATE

TRUTH TABLE

A	B	A ⊕ B
0	0	0
0	1	1
1	0	1
1	1	0

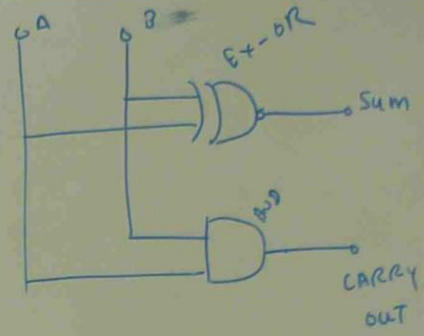
$$\begin{array}{r} 9 \\ +\ 1 \\ \hline 1\ 0 \end{array}$$

↑ CARRY

$$\begin{array}{r|l} 2 & 9 \\ \hline & 4 \end{array}$$

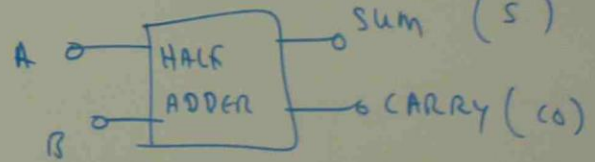
1

HALF ADDER



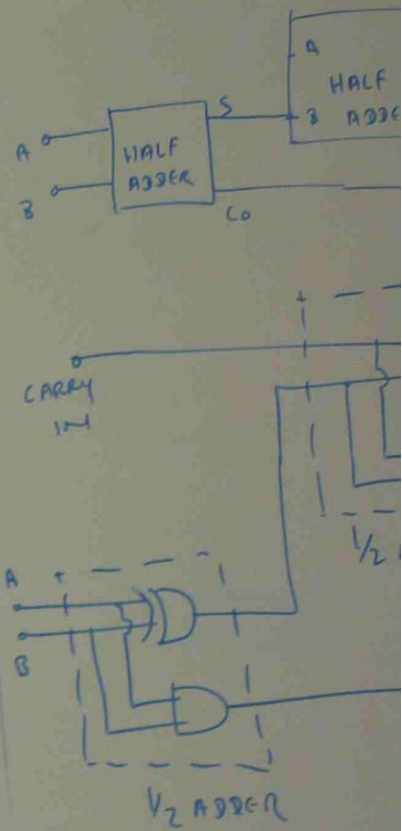
TRUTH TABLE

A	B	SUM	CARRY
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

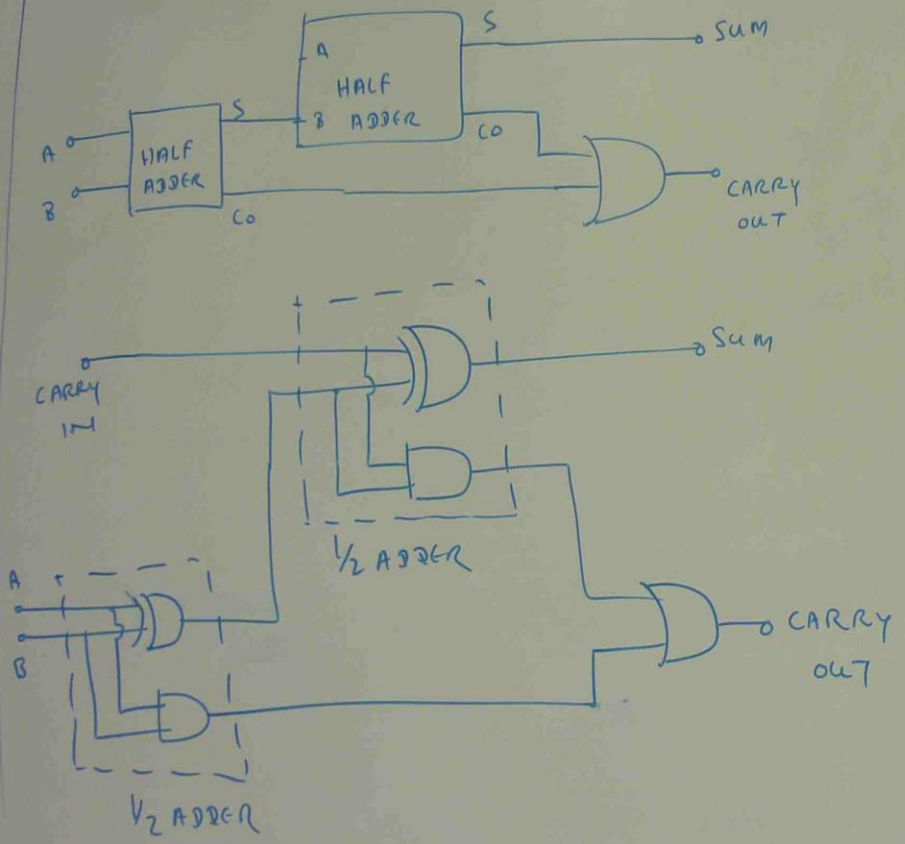


HALF ADDER CAN ONLY ADD TWO BINARY BITS. IT DOES NOT ALLOW FOR A CARRY IN FROM

FULL ADDER



FULL ADDER



TRUTH TABLE OF FULL ADDER

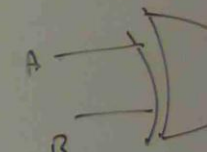
INPUTS			OUTPUTS	
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	1	0	0	1
1	1	1	1	1

FULL ADDER

USE FOR 4 BIT BINARY NUMBER.

EX-OR

A	B	Z
0	0	0
1	0	1
0	1	1
1	1	0



ICs

GATE TYP

AND
OR
NAND
NOR
EX OR

S)

(CO)

ADD TWO

ALLOW FOR A CARRY IN FROM PREVIOUS ADDITION

SUM

CARRY OUT

SUM

CARRY OUT

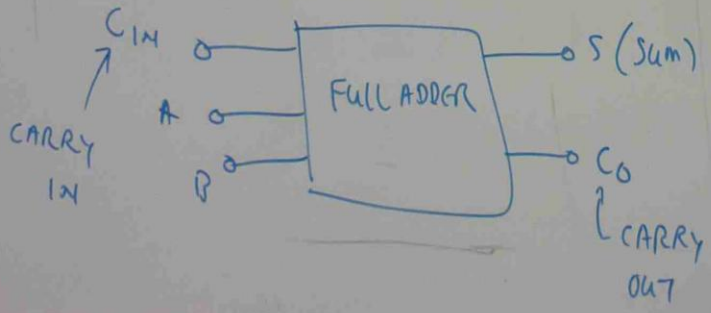
TION

TRUTH TABLE OF FULL ADDER

INPUTS			OUTPUTS	
A	B	CIN	SUM	COUT
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	1	0	0	1
1	1	1	1	1

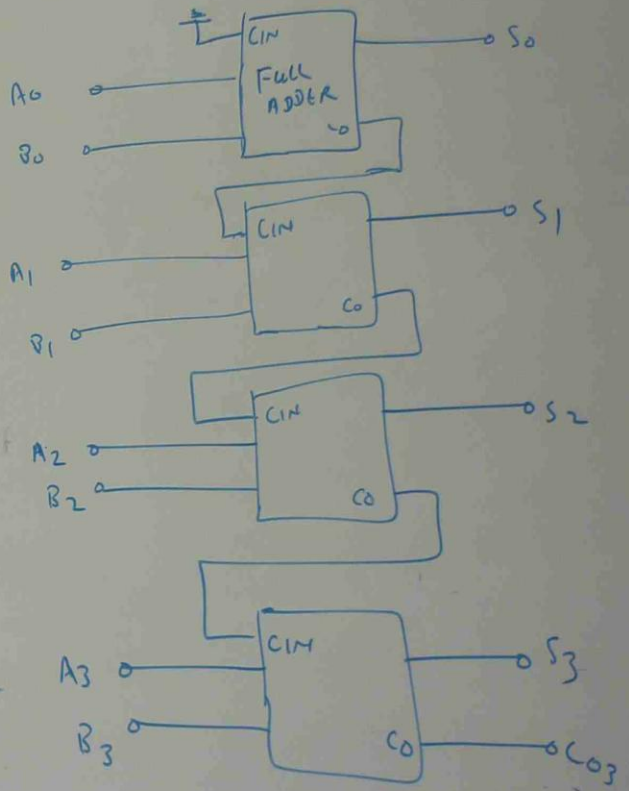
FULL ADDER

USE FOR 4 BIT BINARY NUMBER.



CASCADING

CASCADING 4 FULL ADDERS TO ADD TWO, 4 BIT BINARY NUMBERS.



ENCODERS & DECODERS

ANY DATA WITH IN A DIGITAL CIRCUIT IS COMPRISED of "1S" AND "0S", ALTHOUGH AN OUTPUT DEVICE MAY DISPLAY THE DATA IN VARIOUS FORMS, SUCH AS THE OCTAL (OR) HEXADECIMAL FORM.

IN PUT DEVICES TO A DIGITAL CIRCUIT, SUCH AS KEY BOARD (OR) A DIGITAL TRANSDUCER WILL INPUT THE BINARY INFORMATION IN A FORM OTHER THAN STRAIGHT BINARY : THAT IS, AS A CODE.

TO CHANGE THE BINARY DATA CODES FROM ONE FORM TO ANOTHER, DECODERS AND ENCODERS ARE USED.

DECIM
0
1
2
3
4
5
6
7
8
9

BCD BINARY CODED DECIMAL

$23_{10} = 0010\ 0011$ (BCD)

$2579_{10} = 0010\ 0101\ 0111\ 1001$ (BCD)

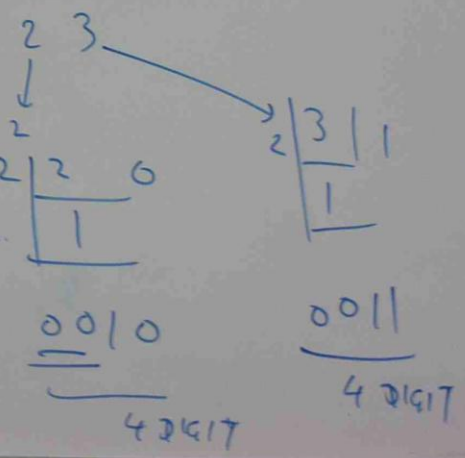
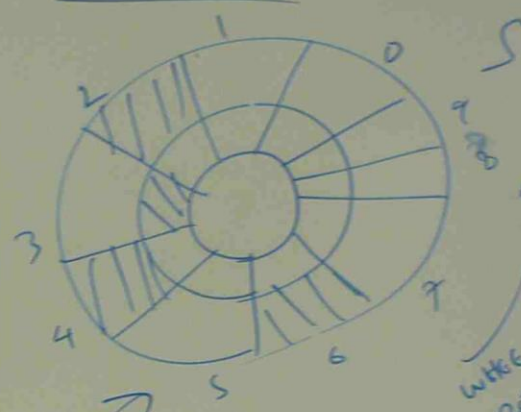


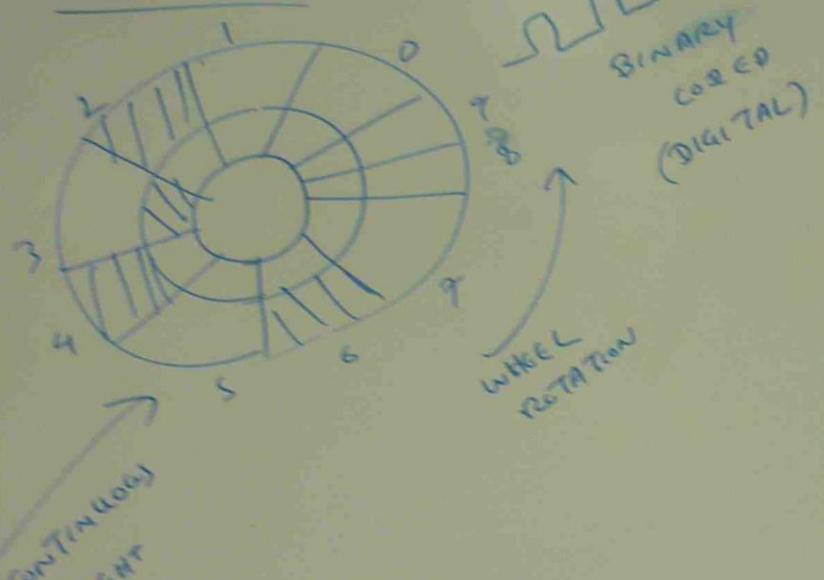
TABLE DECIMAL → BCD

DECIMAL	BCD
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001

GRAY CODE



GRAY CODE



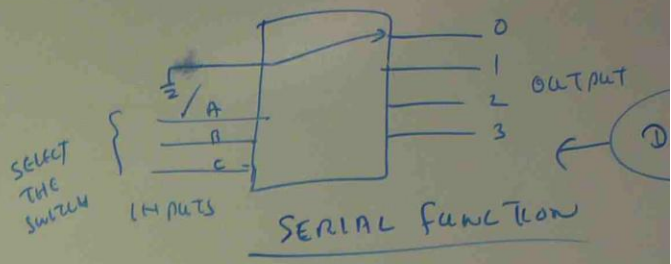
ANALOG

GRAY CODE TABLE

DECIMAL	BINARY	GRAY CODE
0	0000	0000
1	0001	0001
2	0010	0011
3	0011	0010
4	0100	0110
5	0101	0111
6	0110	0101
7	0111	0100
8	1000	1100
9	1001	1101
10	1010	1111
11	1011	1110
12	1100	1010
13	1101	1011
14	1110	1001
15	1111	1000

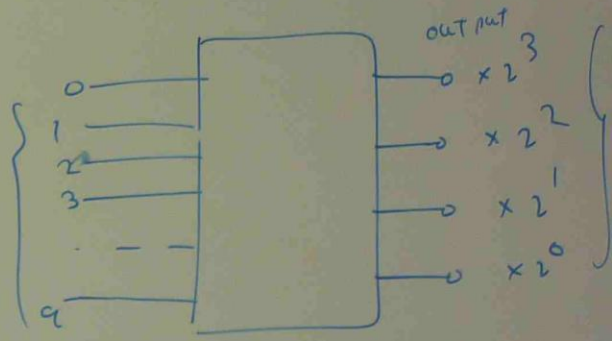
DECODER AND ENCODER

A DECODER IS DEFINED AS A DEVICE THAT HAS A NUMBER of INPUTS AND OUTPUTS, BUT ACTIVATES ONLY ONE OUTPUT FOR A GIVEN INPUT CODE



SERIAL FUNCTION

AN ENCODER IS A DEVICE THAT HAS A NUMBER OF INPUTS AND OUTPUTS BUT PRODUCES A SPECIFIC CODE AT THE OUTPUT WHEN ONLY ONE INPUT AT A TIME IS ACTIVATED.



$1011 \longrightarrow 1\times 2^3 + 0\times 2^2$

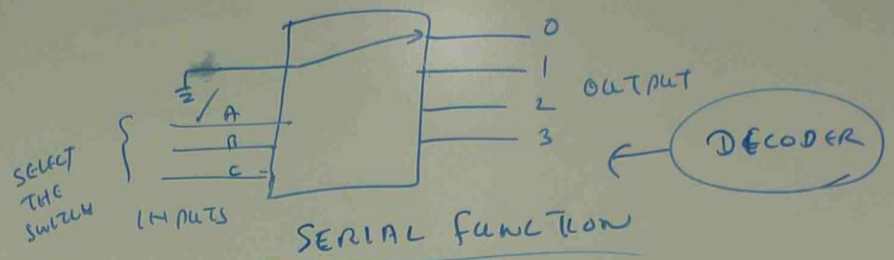
INPUT $= 8 + 0$

$= 11$

PARALLEL FUNCTION

AS A DEVICE THAT HAS A NUMBER OF

BUT ACTIVATES ONLY ONE OUTPUT FOR

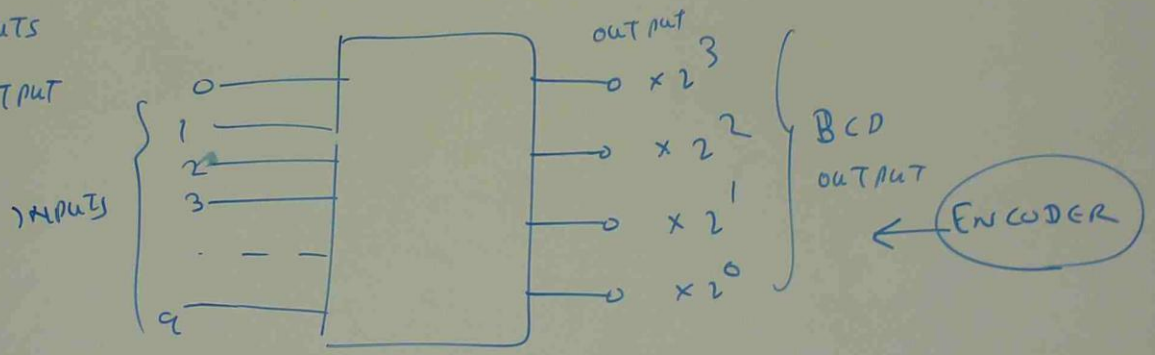


SERIAL FUNCTION

CE THAT HAS A NUMBER OF INPUTS

RODUCES A SPECIFIC CODE AT THE OUTPUT

AT A TIME IS ACTIVATED.



$1011 \longrightarrow 1\times2^3+0\times2^2+1\times2^1+1\times2^0$

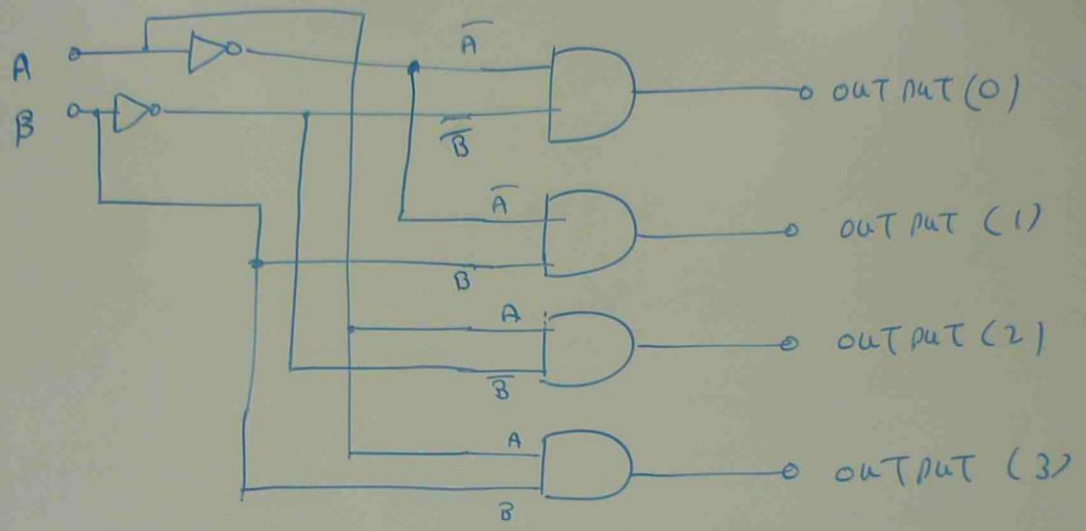
INPUT

$= 8+0+2+1$

PARALLEL $= 11$

FUNCTION

CONSTRUCTING A DECODER BY DIGITAL GATES



THERMO COUPLES

TYPE	MATERIAL (+)	MATERIAL (−)	ΔV/°C AT 100°C (μV)	USABLE RANGE (°C)	COMMENT
E	CHROMEL (90% NICKEL, 10% CHROMIUM)	CONSTANTAN (57% COPPER, 43% NICKEL)	68	0 TO 800	HIGHEST OUTPUT THERMO COUPLE
T	COPPER	CONSTANTAN	46	−185 TO +300	USED FOR MILDLY OXIDISING ATMOSPHERE
K	CHROMEL	ALUMEL 94% NICKEL, 3% MANGANESE 2% ALUMINIUM 1% SILICON	42	0 TO 1100	GENERAL PURPOSE WIDELY USED
J	IRON	CONSTANTAN	46	20 TO 700	USED WITH REDUCING ATMOSPHERE
R/S	PLATINUM/13% RHODIUM PLATINUM		8	0 TO 1600	HIGH TEMPERATURE
V/U	COPPER	COPPER/NICKEL	—	—	COMPENSATING CABLE UP TO 50°C

	COMMENT
	HIGHEST OUT PUT THERMO COUPLE
	USED FOR MILDLY OXIDISING ATMOSPHERE
	GENERAL PURPOSE WIDELY USED
	USED WITH REDUCING ATMOSPHERE
O	HIGH TEMPERATURE
	COMPENSATING CABLE UP TO 50°C

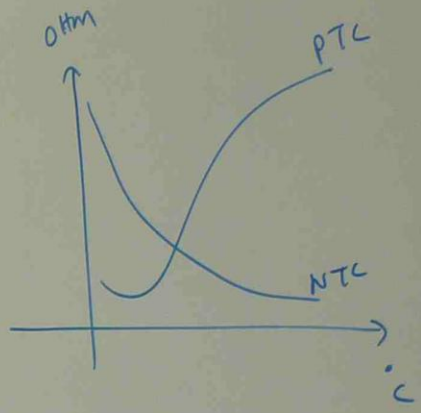
THERMISTOR

THESE ARE TEMPERATURE DEPENDENT RESISTORS. THEIR RESISTANCE IS DETERMINED BY THEIR TEMPERATURE.

TWO BASIC TYPES

PURE METAL

METAL OXIDE



PURE METAL

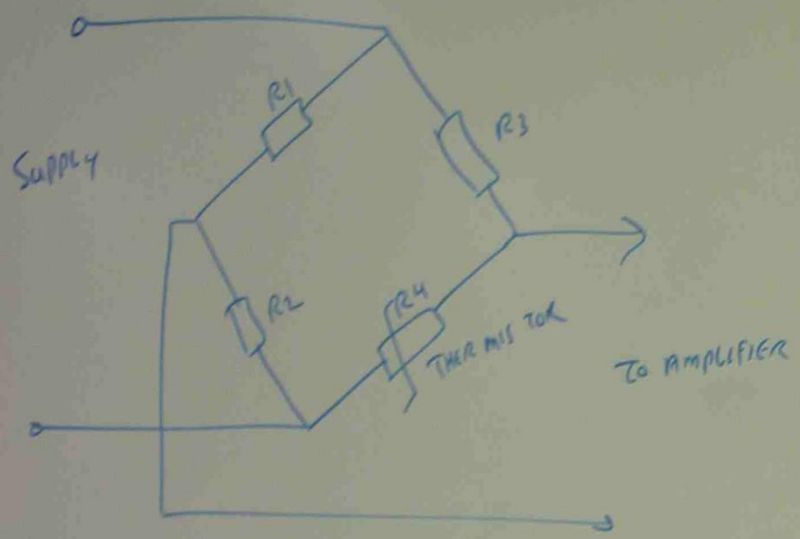
RESISTANCE TEMPERATURE DETECTOR (RTD).

METAL OXIDE

→ POSITIVE TEMPERATURE COEFFICIENT (PTC)
RESISTANCE DECREASES FOR A TEMPERATURE DECREASES

→ NEGATIVE TEMPERATURE COEFFICIENT (NTC)
RESISTANCE DECREASES FOR A TEMPERATURE INCREASES

RESISTANCE RANGE FOR THERMISTOR	10Ω → 1MΩ (STANDARD)	100Ω → 100KΩ (MEASUREMENT)	REFERENCE RESISTANCE OHMS AT 25°C



ADVANTAGES

SMALL SIZE

FAST RESPONSE

DISADVANTAGES

POOR LINEARITY

LIMITED RANGE

APPLICATIONS

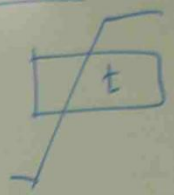
MOTOR PROTECTION

TEMPERATURE MONITORING

MEAT COOKING SENSING

ENGING EXHAUST TEMPERATURE SENSING

RTD



THE RESISTANCE TEMPERATURE DETECTOR IS A PURE METAL THERMISTOR. THEY HAVE A POSITIVE TEMPERATURE COEFFICIENT (PTC).

INDUSTRIAL STYLE THERMISTORS ARE OFTEN CONSTRUCTED IN A STAINLESS STEEL SHEET TO PROTECT THE EXPENSIVE DETECTORS.