ENCODERS AND DECODER

SERIAL DATA

A DATA TRANSFER METHOD IN WHICH EACH BIT IS FED SEQUENTIALLY OVER A SINGLE TRANSMISSION LINE

PARALLEL DATA

A DATA TRANSFER METHOD WHERE DATA IS TRANSFERRED OVER A NUMBER OF LINES.

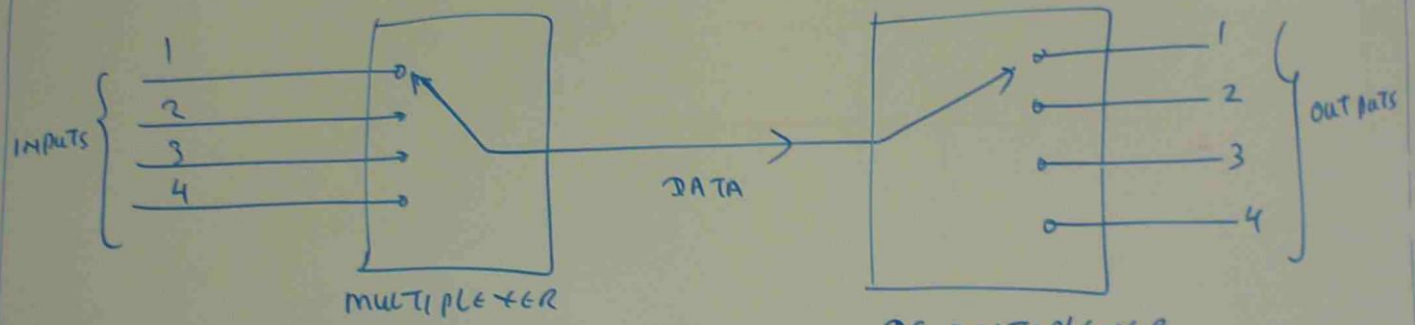
ASCII CODE (AMERICAN STANDARD CODE FOR INFORMATION INTERCHANGE)

- 7 BIT CODE FOR ALL ALPHA NUMERIC CHARACTERS ON TYPE WRITER.
- USED FOR SENDING TEXT BETWEEN COMPUTERS, PRINTERS, WORD PROCESSORS ETC.

CHARACTER	ASCII CODE	
	BINARY	HEX
A	100 0001	41
B	100 0010	42
a	110 0001	61
0	011 0000	30
9	011 1001	39
SPACE	010 0000	20

MULTIPLEXERS

A SPECIAL USE OF DECODER / ENCODER ICS IS MULTIPLEXING WHICH, IN AN ELECTRICAL SENSE, MEANS USING ONE DATA LINE TO TRANSMIT SEVERAL SIGNALS; APPARENTLY SIMULTANEOUSLY.



MULTIPLEXER
(DATA SELECTOR)

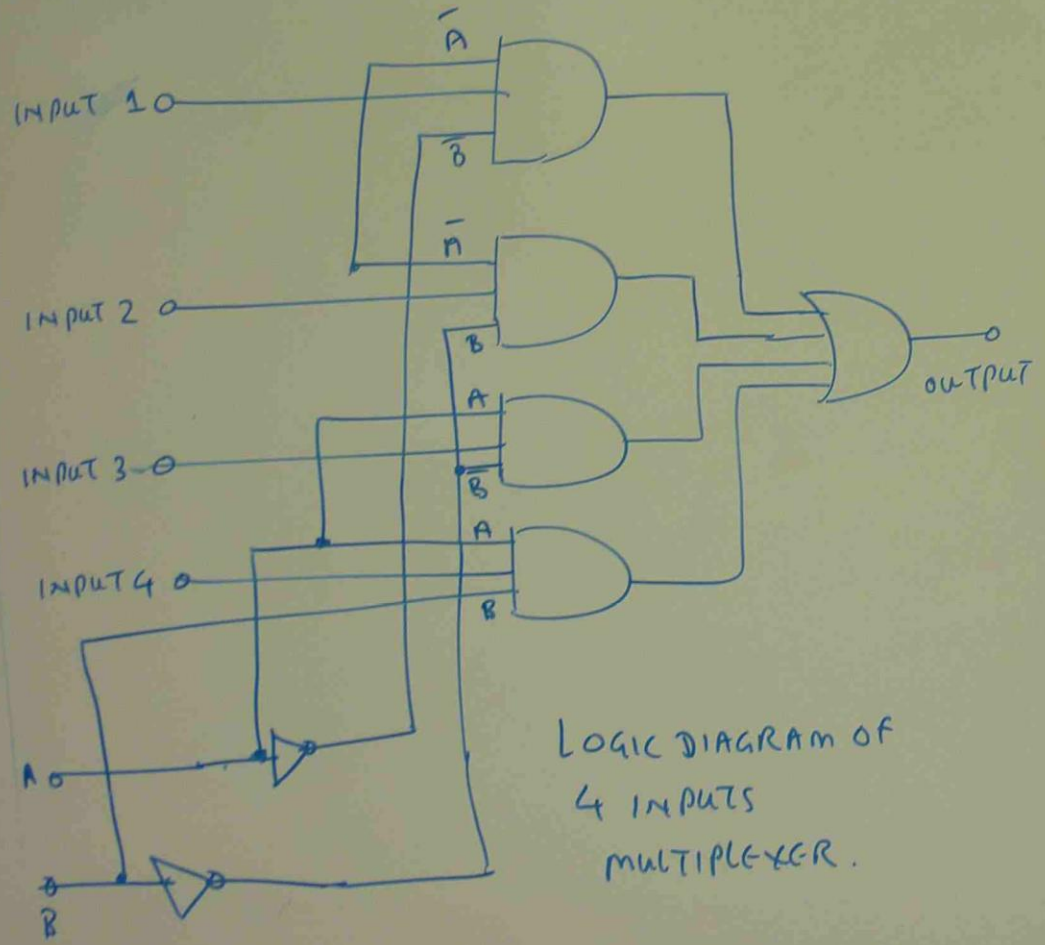
DE MULTIPLEXER
(DATA DISTRIBUTOR)

(4 POLES SINGLE WAY SWITCH)

MULTIPLEXING IS OFTEN USED IN COMPUTERS TO TRANSMIT DATA OVER A SINGLE LINE. (Eg. PRINTED CIRCUIT BOARD TRACK)

MULTIPLEXER (DATA SELECTOR)

– A FORM OF ENCODER

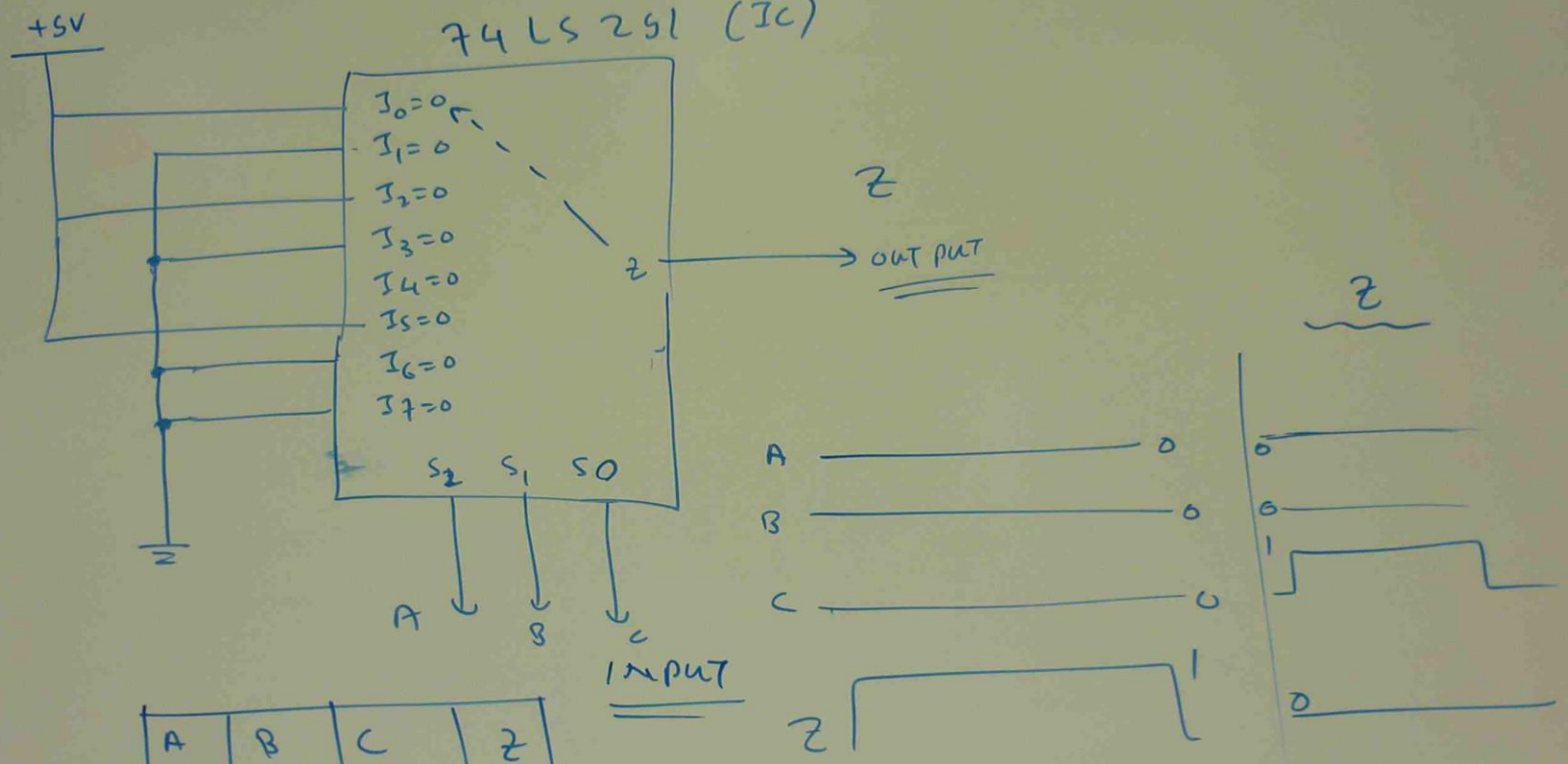


LOGIC DIAGRAM OF 4 INPUTS MULTIPLEXER.

MULTIPLEXER IC

TYPE	DEVICE	OUTPUT	
QUAD 2 INPUT	74LS157	TRUE	
QUAD 2 INPUT	74LS158	OUTPUT INVERTED	
QUAD 2 INPUT	74LS257	TRUE	
QUAD 2 INPUT	74LS258	INVERTED	
QUAD 2 INPUT	74LS298	LATCHED	
DUAL 4 INPUT	74LS153	TRUE	
DUAL 4 INPUT	74LS253	TRUE	
DUAL 4 INPUT	74LS352	INVERT	
DUAL 4 INPUT	74LS353	INVERT	
8 INPUT	74LS151	INVERT + TRUE	
8 INPUT	74LS251	INVERT	+ TRUE
8 INPUT	74LS152	INVERT	
16 INPUT	74150	INVERT	

TRANSFERRING DIGITAL DATA ALONG A COMMON DATA LINE → USE MULTIPLEXER



A	B	C	Z
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	1	0	0
1	1	1	0

FLIP FLOP

COMBINATIONAL LOGIC – MULTIPLEXER / DE-MULTIPLEXER (NO MEMORY)

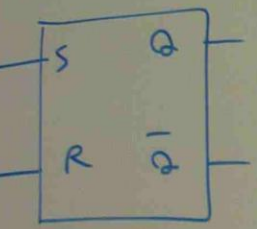
OUTPUT REMAINS STEADY AS LONG AS INPUT CONDITIONS REMAIN CONSTANT

SEQUENTIAL LOGIC – UTILIZE MEMORY DEVICE

SEQUENTIAL DIGITAL SYSTEM.

FUNDAMENTAL ELEMENT of SEQUENTIAL LOGIC IS FLIP FLOP

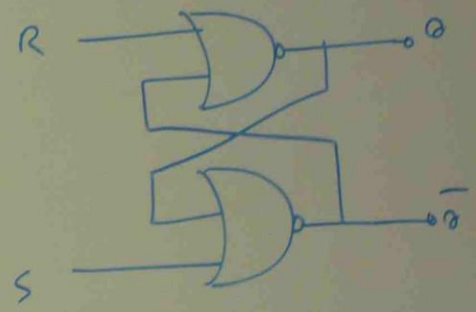
INPUT | OUTPUT | SET/RESET DEVICE (SR)



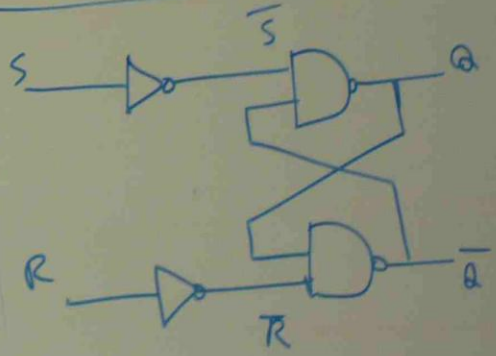
TRUTH TABLE

INPUTS		OUTPUT		RESULT
S	R	Q	$\bar{Q}$	
INACTIVE	INACTIVE	X	X	NO CHANGE
ACTIVE	INACTIVE	1	0	SET
INACTIVE	ACTIVE	0	1	RESET
ACTIVE	ACTIVE	UNDEFINED		INVALID

NOR GATE S R FLIP FLOP



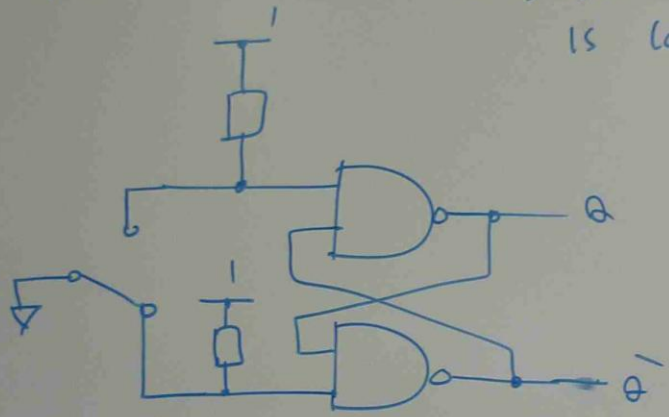
NAND GATE SR FLIP FLOP



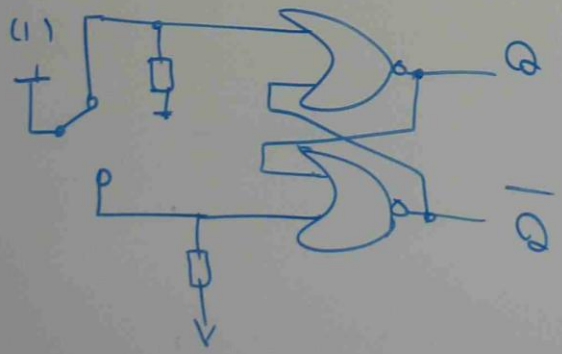
NAND RS FLIP FLOP TO DE BOUNCE SWITCH

SINGLE POLE DOUBLE THROW TYPE (SPDT)

PULL UP RESISTORS ⟶ OPEN CIRCUIT INPUT IS LOGIC 1



DE BOUNCING SWITCH WITH NAND GATE

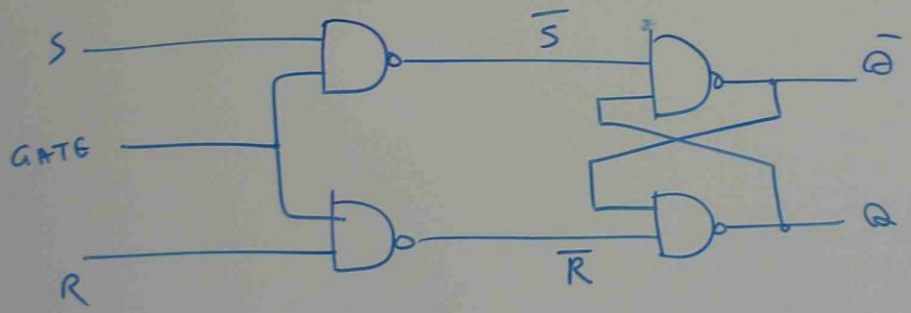


DE BOUNCING SWITCH WITH NOR GATE

GATED SR LATCH ⟶ CLOCKED R S FLIP FLOP

THE BASIC SR FLIP FLOP RESPONDS TO ITS INPUTS DIRECTLY WHICH IN MANY INSTANCES CAUSE TIMING PROBLEMS.

TO OVERCOME THIS IS A CLOCKED SR FLIP FLOP USED TO STORE THE DATA. (STATE OF THE SET (OR) RESET TERMINALS) ONLY WHEN THE FLIP FLOP IS ENABLED BY ANOTHER SIGNAL CALLED CLOCK SIGNAL.



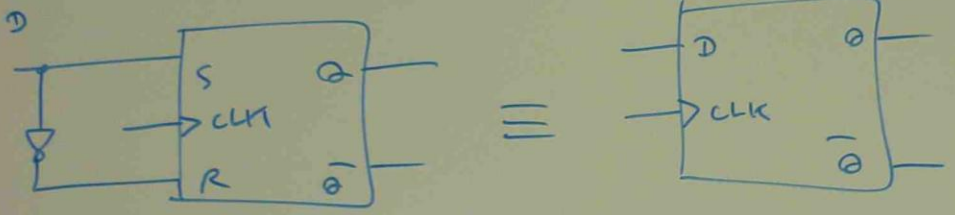
THE SR DATA IS PASSED ONTO FLIP FLOP ONLY WHEN THE GATE (OR) ENABLE SIGNAL IS A LOGIC 1. THE FLIPFLOP WILL STORE THE R S DATA EXISTING AT THE INSTANT THE ENABLE SIGNAL IS REMOVED.

DEVELOPMENT OF FLIP FLOP

SR FLIP FLOP IS NOT A COMMONLY USED DEVICE BECAUSE IT HAS INVALID STATE.

D, T, K FLIP FLOPS ARE DEVELOPED TO OVERCOME THE PROBLEM

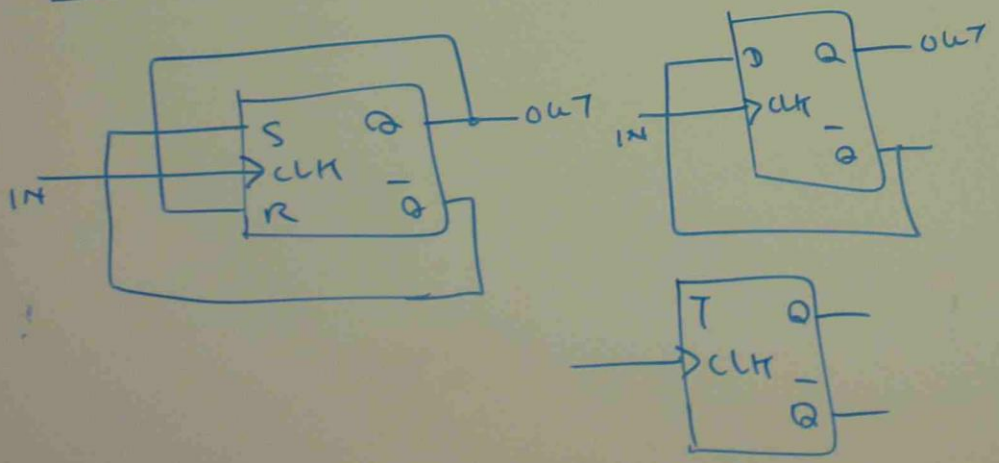
D FLIP FLOP



D FLIP FLOP TRUTH TABLE

	D	Q_n	Q_{n+1}	
1	0	0	0	RESET
2	0	1	0	
3	1	0	1	SET
4	1	1	1	

TOGGLE (T) FLIP FLOP



J-K FLIP FLOP

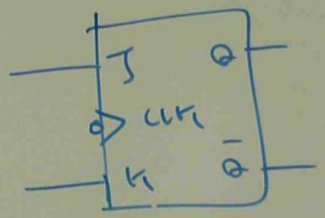
THE J-K FLIP FLOP OVERCOMES THE PROBLEM OF THE POSSIBLE INVALID OUTPUT CONDITION IN S-R FLIP FLOP WHILE STILL RETAINING TWO INPUTS.

THE SET INPUT IS NOW J INPUT. THE RESET INPUT IS NOW THE K INPUT.

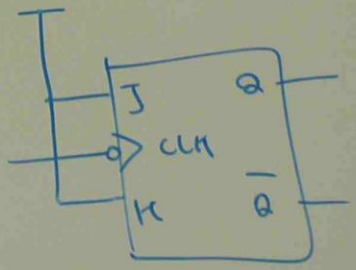
IF BOTH THE J AND K INPUTS ARE HELD AT A LOGIC 1, THE OUTPUTS WILL TOGGLE RATHER THAN BECOME INDETERMINE

JK FLIP FLOP TRUTH TABLE

	J	K	Q	Q$_{n+1}$	
1	0	0	0	0	NO CHANGE
2	0	0	1	1	
3	0	1	0	0	RESET
4	0	1	1	0	
5	1	0	0	1	SET
6	1	0	1	1	
7	1	1	0	1	TOGGLE
8	1	1	1	0	

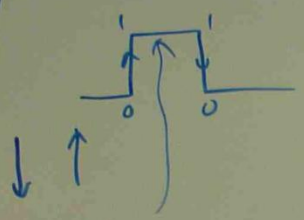


JK FLIP FLOP
(NEGATIVE EDGE TRIGGERED)



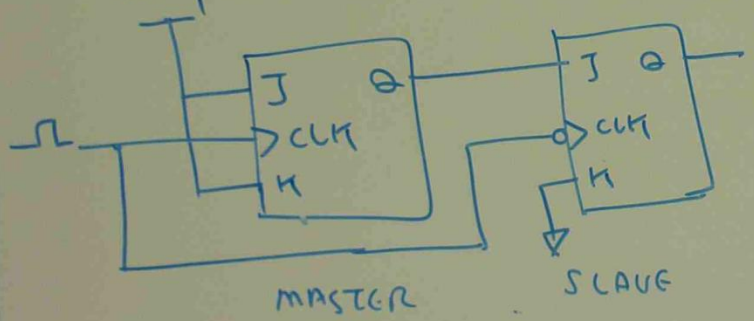
T FLIP FLOP FROM JK FLIP FLOP

MASTER - SLAVE FLIP FLOP



CONNECTING CONVENTIONAL J-K FLIP FLOP CAN GIVE THE PROBLEMS DUE TO TIME DELAY

THE PROBLEMS CAN ARISE FROM THE FACT THAT ALTHOUGH THE FLIP FLOP CHANGES ON THE EDGE OF IT'S CLOCK SIGNAL, THERE IS A SMALL TIME INTERVAL BEFORE AND AFTER THE CLOCK EDGE DURING WHICH THE INPUT DATA MUST BE HELD STABLE. THESE TIMES ARE CALLED SET UP & HOLD TIMES RESPECTIVELY.



WHEN THE CLOCK IS HIGH

MASTER IS ENABLED) SLAVE IS DISABLED

MASTER OUTPUT WILL BE SET ACCORDING TO DATA PRESENTS AT MASTER'S INPUT) SLAVE FLIP FLOP REMAINS UNCHANGED

WHEN THE CLOCK SIGNAL RETURNS TO ZERO

SLAVE FLIP FLOP WILL RESPOND TO THE OUTPUT OF MASTER.

TRUTH DIAGRAMS OF EDGE TRIGGERED FLIP FLOP AND MASTER SLAVE FLIP FLOP

INPUT			OUTPUT	
CLK	J	K	Q	$\bar{Q}$
↓	L	L	Q_0	$\bar{Q}_0$
↓	H	L	H	L
↓	L	H	L	H
↓	H	H	TOGGLE	

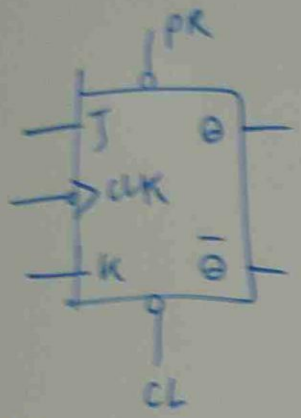
EDGE TRIGGERED FLIP-FLOP

INPUT			OUTPUT	
CLK	J	K	Q	$\bar{Q}$
⊓	L	L	Q_0	$\bar{Q}_0$
⊓	H	L	H	L
⊓	L	H	L	H
⊓	H	H	TOGGLE	

MASTER-SLAVE FLIP FLOP

ANGED

JK FLIP FLOP WITH ASYNCHRONOUS PRESET AND CLEAR



PR - PRESET

CL - CLEAR

INPUTS					OUTPUTS	
PR	CL	CLK	J	K	Q	$\bar{Q}$
L	H	X	X	X	H	L
H	L	X	X	X	L	H
L	L	X	X	X	H*	H*
H	H	↓	L	L	Q_0	$\bar{Q}_0$
H	H	↓	H	L	H	L
H	H	↓	L	H	L	H
H	H	↓	H	H	TOGGLE	
H	H	H	X	X	Q_0	$\bar{Q}_0$

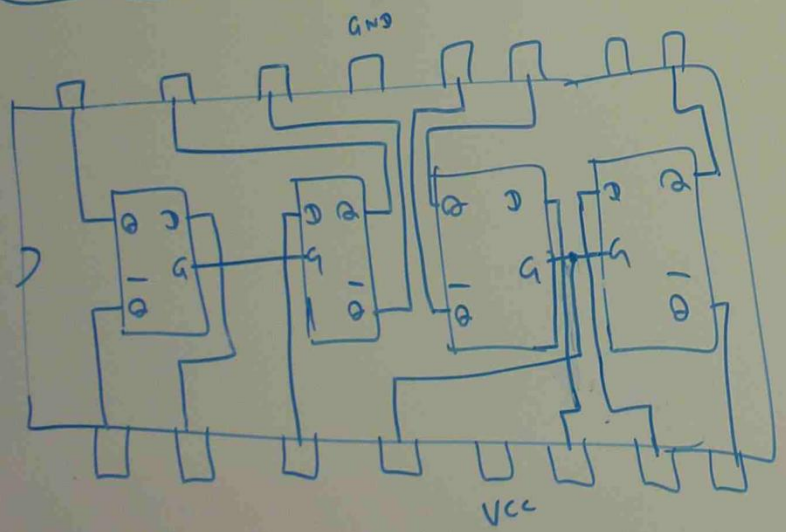
SHIFT REGISTERS AND DATA LATCHES

FLIP FLOPS ARE USED IN A VARIETY OF APPLICATIONS INCLUDING THE LATCH AND SHIFT REGISTER FUNCTIONS.

- FLIP FLOP → STORE 1 BIT OF DATA

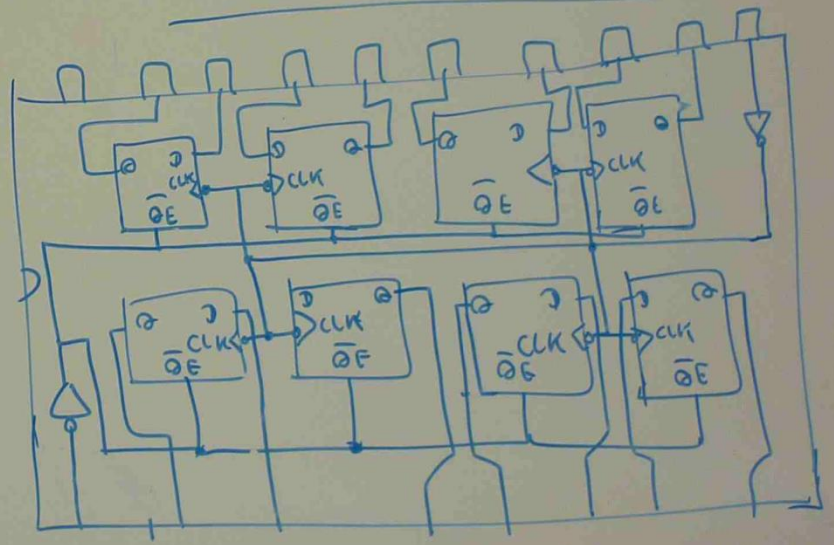
LATCH → INTER CONNECTION OF FLIP FLOPS → CAN STORE SEVERAL BITS OF DATA

4 BIT LATCH → 4 FLIP FLOP – STORE 4 BIT DATA



74 LS 75 4 BIT LATCH

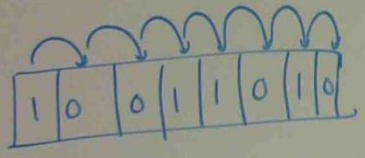
8 BIT LATCH – STORE 8 BIT DATA



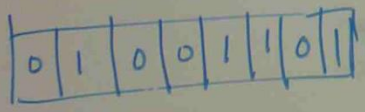
74 LS 374 OCTAL D TYPE LATCH

SHIFT REGISTERS

MANY DIGITAL APPLICATIONS REQUIRE THAT BINARY DATA BE SHIFTED EITHER TO LEFT (OR) RIGHT

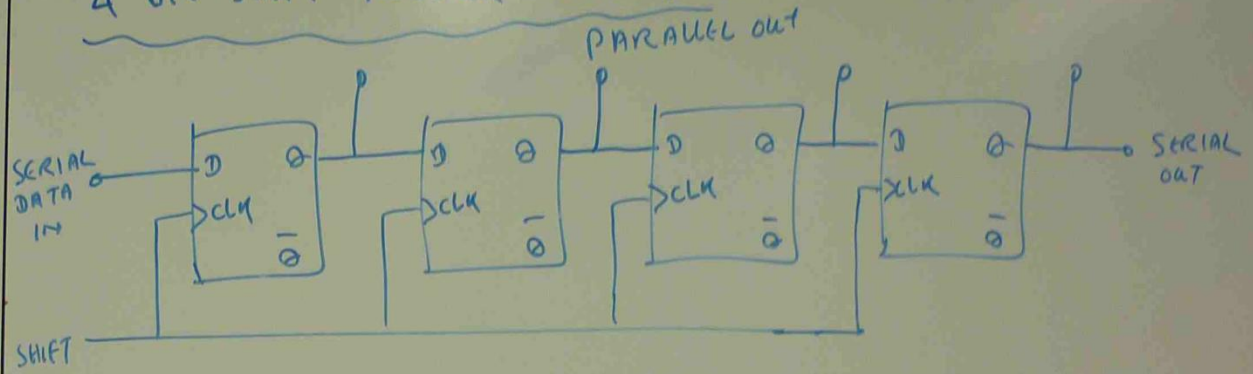


154_{10}

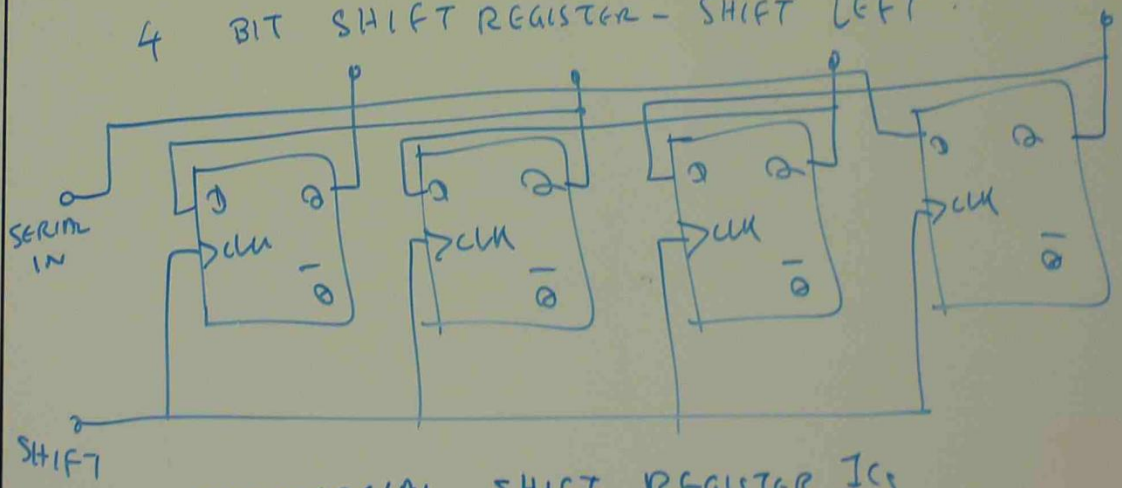


77_{10}

4 BIT SHIFT REGISTER – SHIFT RIGHT



4 BIT SHIFT REGISTER – SHIFT LEFT



COMMERCIAL SHIFT REGISTER ICs

TTL 74LS194, CMOS 4194 } (16 PIN 4 REGISTERS)

COUNTERS

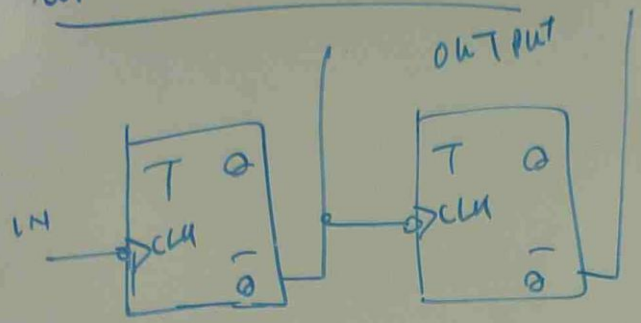
- COUNTERS CAN BE USED TO COUNT THE NUMBER OF ITEMS ON A CONVEYOR (OR) IF USED TO COUNT THE NUMBER OF PULSES FROM A SHAFT ENCODER CAN INDICATE THE ROTARY POSITION OF A SHAFT (OR) X-Y POSITION OF MACHINING BEDS
- FLIP FLOPS ARE CONNECTED AS COUNTERS
- COUNTER PRODUCES A SERIES OF BINARY NUMBERS STARTING AT A PRESET VALUE (OFTEN 0) CYCLING AT A RATE DETERMINED BY THE INPUT CLOCK.

DECIMAL	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

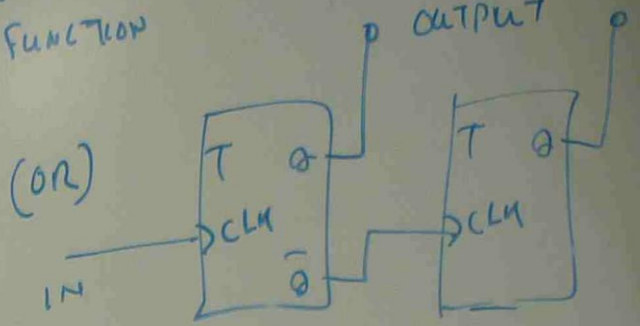
(LSB - LEAST SIGNIFICANT BIT)

3 BITS BANARY COUNTER

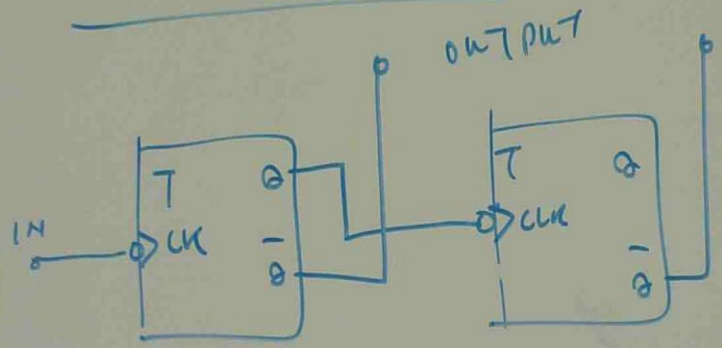
UP COUNTER 0 1 2 3



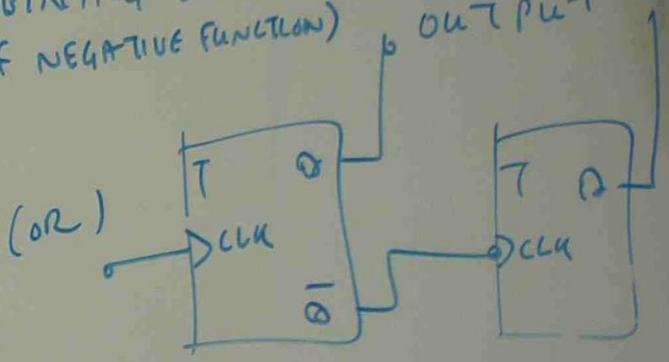
COMBINING ODD NUMBER OF NEGATIVE FUNCTION



DOWN COUNTER 3 2 1 0



(COMBINING EVEN NUMBER OF NEGATIVE FUNCTION)

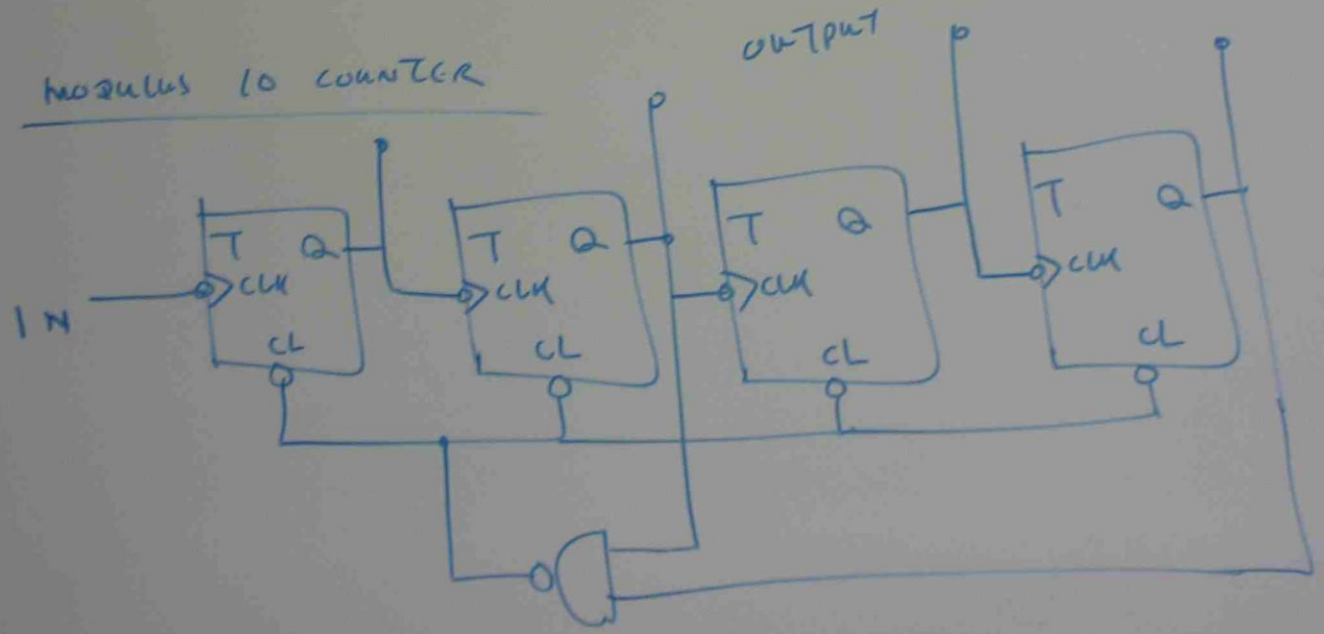


MODULUS of A COUNTER

THE MODULUS of A COUNTER REFERS TO THE NUMBER of THE STATES THAT THE COUNTER CAN OUTPUT

0 ⟶ 15 COUNTER HAS 16 STATES. IT IS MODULO 16 COUNTER

MODULUS 10 COUNTER

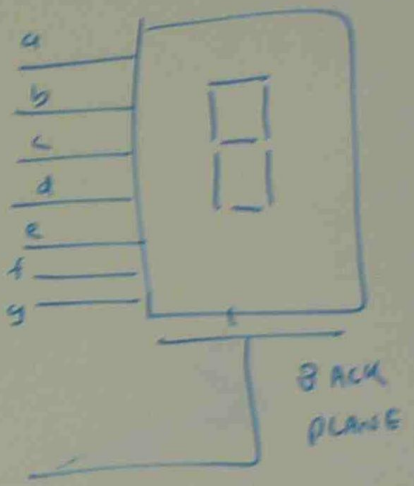


COUNTER ICS

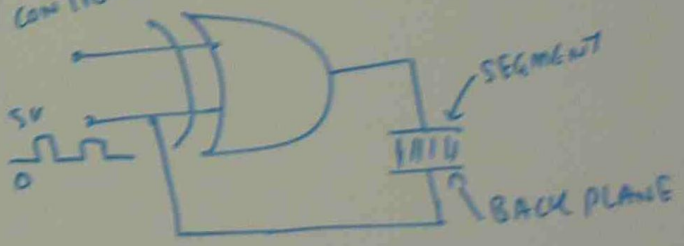
TYPE	MODULUS	CLOCK FREQUENCY
74LS90	2 x 5	32 MHz
74LS92	2 x 6	32 MHz
74LS93	2 x 8	32 MHz
74LS390	2 x 5	40 MHz
4020	16384	10 MHz
4024	128	12 MHz

7 SEGMENT DISPLAY

LCD DISPLAY

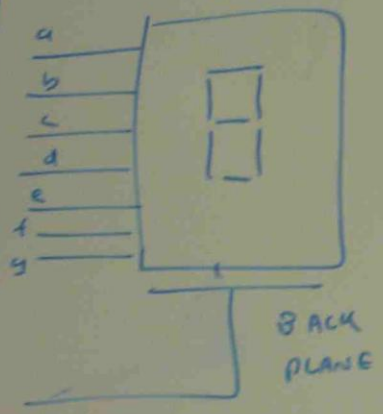


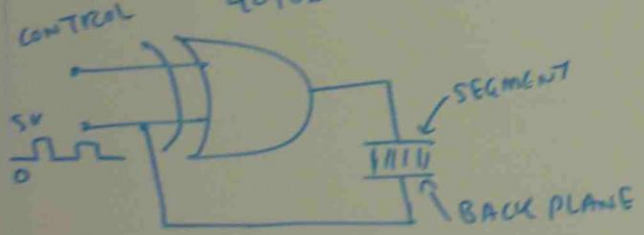
4070B



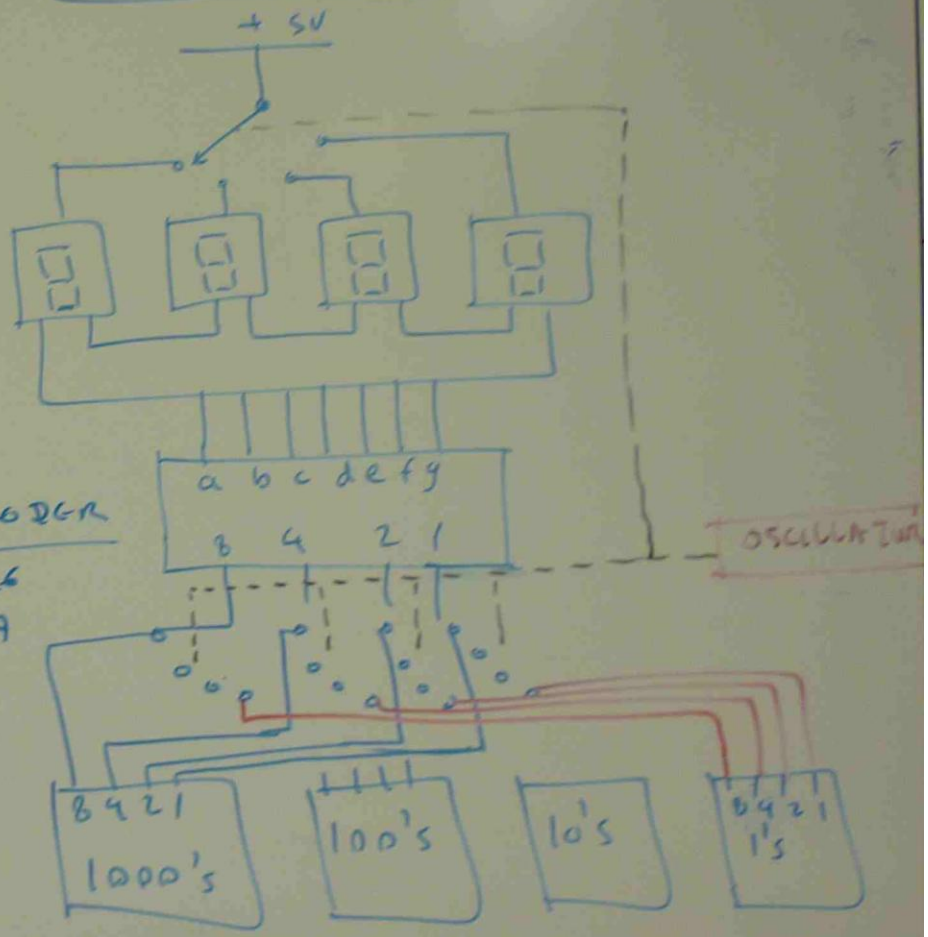
7 SEGMENT DISPLAY

LCD DISPLAY



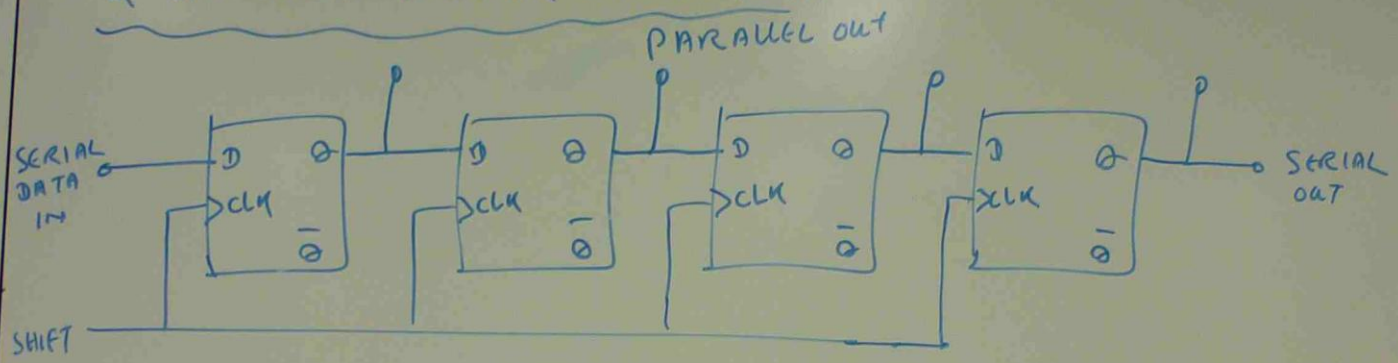


MULTIPLEXED LCD DISPLAY

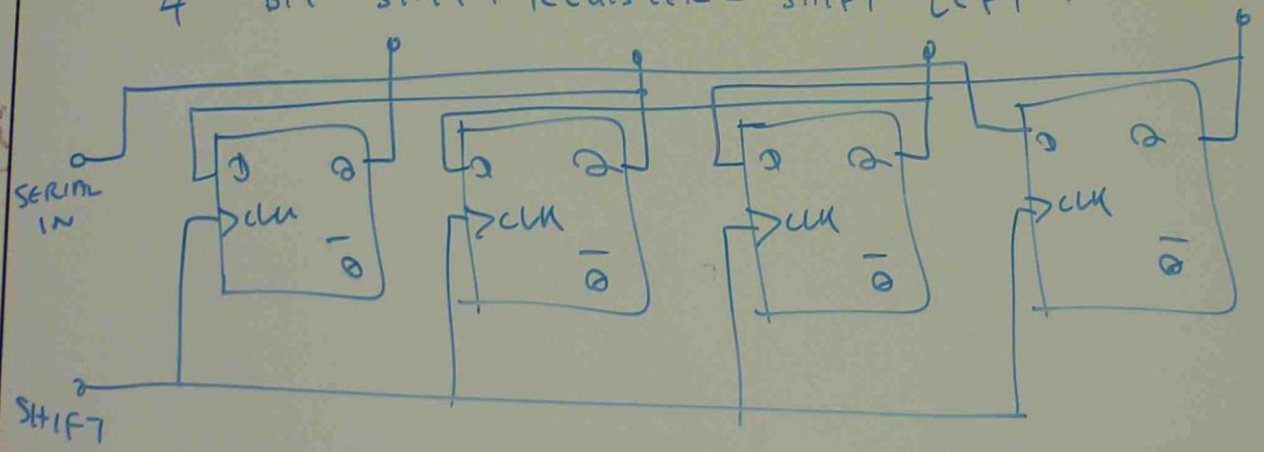


MULTIPLEXING 7 SEGMENT LCD DISPLAY.

4 BIT SHIFT REGISTER – SHIFT RIGHT



4 BIT SHIFT REGISTER – SHIFT LEFT



COMMERCIAL SHIFT REGISTER ICs

TTL 74LS194, CMOS 4194 } (16 PIN 4 REGISTERS)

COUNTERS

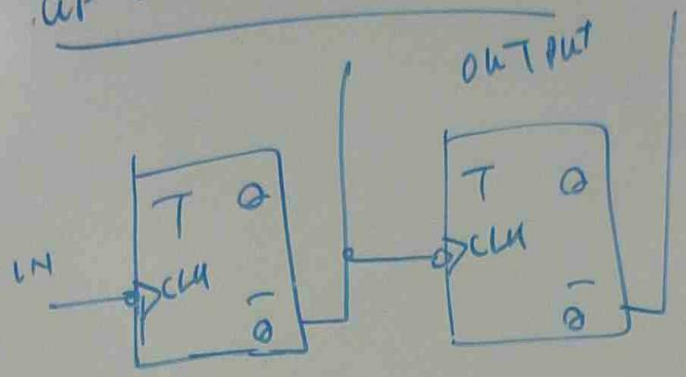
- COUNTERS CAN BE USED TO COUNT THE NUMBER OF ITEMS ON A CONVEYOR (OR) IF USED TO COUNT THE NUMBER OF PULSES FROM A SHAFT ENCODER CAN INDICATE THE ROTARY POSITION OF A SHAFT (OR) X–Y POSITION OF MACHINING BEDS
- FLIP FLOPS ARE CONNECTED AS COUNTERS
- COUNTER PRODUCES A SERIES OF BINARY NUMBERS STARTING AT A PRESET VALUE (OFTEN 0) CYCLING AT A RATE DETERMINED BY THE INPUT CLOCK.

DECIMAL	C	B	A
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1

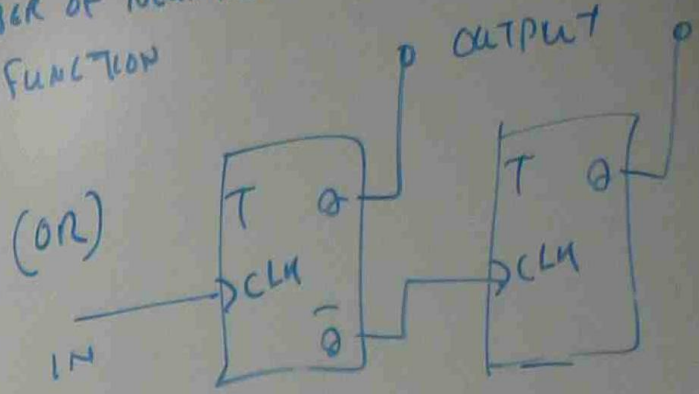
(LSB - LEAST SIGNIFICANT BIT)

3 BITS BANARY COUNTER

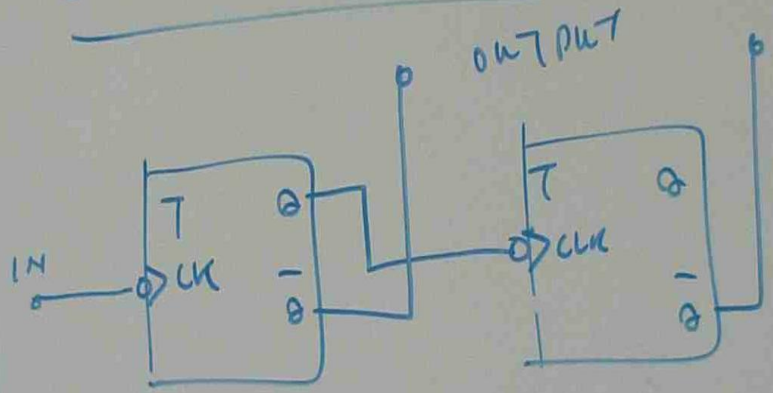
UP COUNTER 0 1 2 3



COMBINING ODD NUMBER OF NEGATIVE FUNCTION



DOWN COUNTER 3 2 1 0



(COMBINING EVEN NUMBER OF NEGATIVE FUNCTION)